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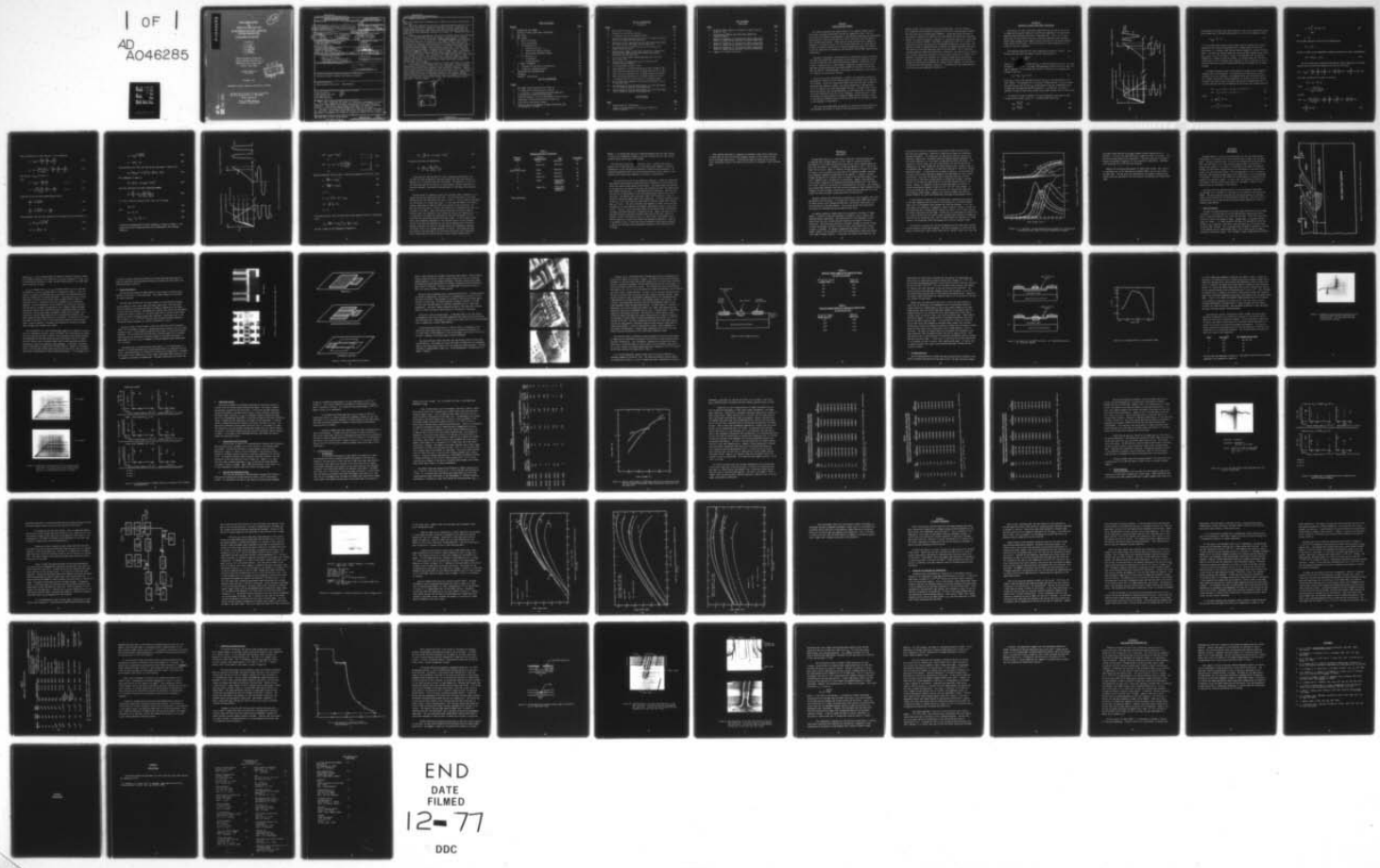

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GALLIUM ARSENIDE FIELD EFFECT TRANSISTORS WITH SEMI-INSULATED GATES

20 June 1975 - 31 July 1977

Prepared By

D. W. Shaw
D. J. Coleman, Jr.
H. M. Macksey
D. N. McQuiddy
V. Sokolov
R. E. Williams

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75222

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This report summarizes the results of a program for development and evaluation of gallium arsenide field effect transistors with semi-insulated gates (SIGFETs). These devices are potentially applicable to a number of microwave systems, including active-element phased-array radars and ECM jammers.

Included in the scope of the program was an analysis of Class A and Class B FET amplifiers; design, fabrication, and dc and rf characterization of SIGFETs; evaluation of procedures for formation of n^{+} contact regions for FETs; and an →

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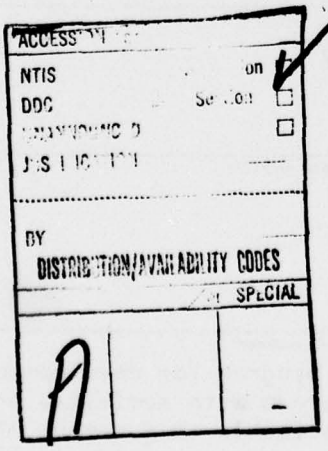
objective comparison of the properties of SIGFETs with those of conventional GaAs FETs.

Theoretical analyses of the dc and rf operating characteristics of Class A and Class B FET amplifiers showed that maximum efficiency is expected for Class B operation into a tuned load. This conclusion was supported by the experimental observation that maximum efficiency was obtained for GaAs FETs when the gate bias approaches the pinch-off voltage, i.e., approaching Class B operation.

Procedures were developed for fabrication of SIGFETs using either epitaxial growth or ion bombardment to form the region of high resistivity or semi-insulating GaAs to be located beneath the gate contact metal. By bombardment with 30 keV argon ions at a dose of 1×10^{14} cm^{-2}, a semi-insulating region is formed that extends 0.2 μm below the surface. SIGFETs fabricated by this procedure were compared with conventional FETs (without semi-insulated gates) fabricated from the same starting material. The SIGFETs have higher gate reverse breakdown voltages, lower transconductances, and ~ 1 dB lower small signal gains. Furthermore, in comparison with conventional FETs, the power saturation of SIGFETs occurs at greater drain voltages. Under cw conditions, the best SIGFET with a 2400 μm gate delivered a maximum output power of 2.7 W with 4 dB gain at 8 GHz. This represents the highest power per unit gate width yet reported for FETs of this size at 8 GHz; it does not, however, differ greatly from the best values reported for the much more widely investigated conventional devices. At 11 GHz a 2400 μm gate width SIGFET yielded 1.1 W output power with 4 dB gain.

To fully exploit the power potential of SIGFETs, techniques for formation of n^+ source/drain contact regions were also investigated. Using localized implantation of selenium or silicon ions with subsequent annealing, enhanced carrier concentrations were produced at the source/drain locations. However, after metallization and alloying, the resulting contacts were no less resistive than alloyed contacts to conventional material of lower carrier concentration. Use of epitaxially grown n^+ layers was examined as an alternate approach. Devices fabricated from this material were found to be capable of withstanding two times more drain voltage before failure than those fabricated without epitaxial n^+ contact regions.



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SECTION I
INTRODUCTION AND SUMMARY

This report summarizes the accomplishments of a research program carried out during a two-year period under Contract No. N00014-75-C-1134. The objective of this program was development of the essential technology for fabrication and evaluation of gallium arsenide field effect transistors with insulated or semi-insulated gate regions. These devices, which are potentially capable of operation in microwave circuits as Class B power amplifiers, are applicable to a number of systems including active element phased-array radars, ECM jammers, and driver amplifiers for terrestrial and satellite line-of-sight communications transmitters.

Included in the scope of this program was a theoretical analysis of Class A and Class B FET amplifiers, development and optimization of procedures for fabrication of GaAs FETs with semi-insulated gates (SIGFETs), evaluation of the dc and rf characteristics of GaAs SIGFETs, comparison of these devices with GaAs FETs having conventional metal gates (MESFETs) fabricated from the same starting material, and development of procedures for formation of low resistivity (n^+) regions for source/drain contacts.

During the course of the program, a reliable ion bombardment process was developed for formation of the localized semi-insulating gate region required for a SIGFET. Using this process GaAs SIGFETs were obtained that yielded outstanding output powers at X-band. One device operating at 8 GHz delivered 2.7 W at 4 dB gain with a 26% power-added efficiency. The gate width of this device was 2400 μm, and the corresponding 1.12 W/mm gate width is the highest value ever reported for any FET at this frequency. Extensive dc and rf characterization of these devices and companion MESFET devices revealed a number of interesting differences and similarities, which will be discussed in detail in the remainder of this report.

The next section describes the analysis of Class A and Class B amplifiers and discusses the results in terms of the relative merits of conventional

MESFETs and FETs with insulated or semi-insulated gates. This is followed by a comparison of the properties expected for FETs with insulated gates (IGFETs) and those with semi-insulated gates (SIGFETs). During the initial portions of the program, procedures for fabrication of both IGFETs and SIGFETs were examined; however, for reasons discussed in Section III, the efforts were later concentrated on the more promising SIGFET. The SIGFET is emphasized in Section IV, where the fabrication process, including the ion bombardment procedures, are detailed. The results of dc and rf characterization of SIGFETs and companion MESFETs fabricated from portions of the same epitaxial material are discussed. The rf comparison includes operation under both pulsed and cw conditions. Low resistivity n^+ source/drain contact regions are believed to be particularly beneficial to SIGFETs; consequently, procedures for formation of n^+ contact regions were also examined during the program. Both localized ion implantation and sequential epitaxial growth were evaluated as procedures for contact region formation, and the results of these efforts are detailed in Section V. The conclusions and recommendations for future work are summarized in Section VI.

SECTION II

ANALYSIS OF CLASS A AND CLASS B AMPLIFIERS

The analysis of Class A and Class B amplifiers was carried out as an aid in comparing the maximum theoretical efficiencies expected for FET amplifiers operating under different bias and rf load conditions. The dc and rf characteristics for both Class A and Class B amplifier operation are considered. Several basic assumptions are made to allow calculation of the maximum possible output power and efficiency. The significances of these assumptions are discussed as they are introduced.

The operating conditions for Class A operation are shown in Figure 1. The equation that describes the dynamic transfer characteristic is

$$I_{ds} = I_{dss} \left(1 + \frac{V_g}{V_p}\right)^2 , \tag{1}$$

where V_p is the pinchoff voltage and I_{dss} is the saturated drain current at a gate voltage of zero ($V_g = 0$). The square law dependence of drain current on gate voltage is apparent. It is assumed that the FET is excited by a sinusoidal gate voltage of the form

$$V_g = -V_{go} + V_{g1} \sin \omega t , \tag{2}$$

where V_{go} is the dc bias applied to the FET and V_{g1} is the amplitude of the rf input signal. The assumption of a sinusoidal voltage waveform is valid provided the amplitude V_{g1} and the bias V_{go} are adjusted so that the instantaneous gate voltage does not exceed the barrier potential ϕ. In addition, for Class A operation the gate voltage cannot exceed the pinchoff voltage (Class A definition).

The maximum rf power obtainable in Class A operation occurs when the gate voltage swings between $-V_p$ and $+\phi$. To achieve these conditions,

$$V_{go} = \frac{V_p - \phi}{2} \quad \text{and} \tag{3a}$$

$$V_{g1} = \frac{V_p + \phi}{2} . \tag{3b}$$

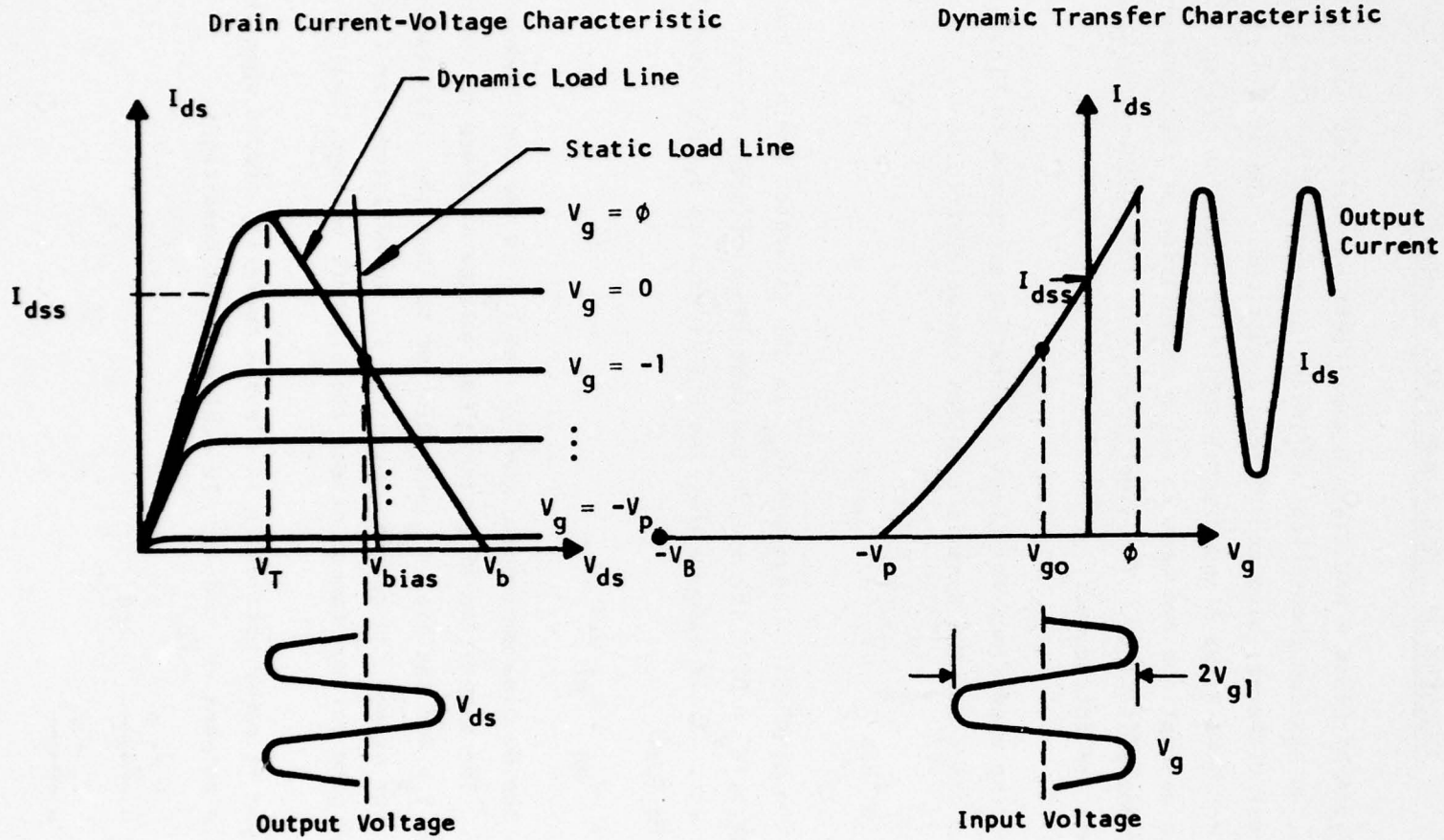


Figure 1 FET Common Source Characteristics (Class A)

The maximum drain voltage that can be applied is set by the reverse bias breakdown voltage (V_B) of the gate Schottky barrier. For Class A operation, then,

$$V_{b_{max}} = V_B - V_p \quad . \tag{4}$$

If it is assumed that maximum rf output power requires maximum drain current modulation, the minimum instantaneous drain voltage cannot be less than V_T (see Figure 1). A dynamic load line can then be assumed for maximum rf output power. The load line passes through the minimum voltage, maximum current point $[V_T, I_{dss}(1 + \phi/V_p)^2]$ as shown in Figure 1 and determines the relationship between the rf output current and voltage. For maximum power and efficiency calculations it will be assumed that a matched rf load is presented to the FET such that the output current is phased 180 degrees with respect to the output voltage.

The power delivered to the rf load consists of power at the fundamental frequency and at the harmonics. The nonlinearity of the dynamic transfer characteristic also introduces a dc component which must be signed properly. The rf power calculation involves expressing the output current and voltage waveforms that result from a sinusoidal excitation of the gate electrode. As a review, consider the Fourier expansion of the current and voltage waveforms

$$I(T) = I_o + I_1 \sin T + J_1 \cos T + I_2 \sin 2T + \ldots \tag{5}$$

$$V(T) = V_o + V_1 \sin T + U_1 \cos T + \ldots \quad , \tag{6}$$

where

$$I_o = \frac{1}{2\pi} \int_o^{2\pi} I(T)\, dT \tag{7}$$

$$I_1 = \frac{1}{\pi} \int_o^{2\pi} I(T) \sin T\, dT \tag{8}$$

$$J_1 = \frac{1}{\pi}\int_0^{2\pi} I(T)\cos T\, dT \qquad (9)$$

etc.,

and

$$T = \omega t \quad .$$

The dc power supplied to the FET can be expressed as

$$P_{dc} = I_o V_o \quad , \qquad (10)$$

and the rf power at the fundamental frequency delivered to a load is expressed as

$$P^1_{rf} = \tfrac{1}{2}(V_1 I_1 + J_1 U_1) \quad . \qquad (11)$$

For the simple case of maximum conditions for Class A operation, the output current can be written from Equations (1) and (2) in the form

$$I(T) = I_{dss}\left[1 - \frac{2V_{go}}{V_p} + \frac{V_{go}^2}{V_p^2} + \tfrac{1}{2}\frac{V_{g1}^2}{V_p^2} + 2\left(1 - \frac{V_{go}}{V_p}\right)\frac{V_{g1}}{V_p}\sin T - \tfrac{1}{2}\frac{V_{g1}^2}{V_p^2}\cos 2T\right]. \qquad (12)$$

The output voltage can be written in the form

$$V(T) = V_b - I(T)\, R_L \quad ,$$

where

$$R_L = \frac{V_b - V_T}{I_{dss}(1 + \phi/V_p)^2} \quad ,$$

so that

$$V(T) = V_b - \frac{(V_b - V_T)}{(1 + \phi/V_p)^2}\left[1 - 2\frac{V_{go}}{V_p} + \frac{V_{go}^2}{V_p^2} + \tfrac{1}{2}\frac{V_{g1}^2}{V_p^2} + 2\left(1 - \frac{V_{go}}{V_p}\right)\frac{V_{g1}}{V_p}\sin T\right.$$

$$\left. - \tfrac{1}{2}\frac{V_{g1}^2}{V_p^2}\cos 2T\right] \quad . \qquad (13)$$

Then, by Equations (7), (8), (9), etc., or by inspection

$$I_o = I_{dss}\left[1 - \frac{2V_{go}}{V_p} + \frac{V_{go}^2}{V_p^2} + \tfrac{1}{2}\frac{V_{g1}^2}{V_p^2}\right] \tag{14}$$

$$V_o = V_b - \frac{(V_b - V_T)}{(1 + \phi/V_p)^2}\left[1 - \frac{2V_{go}}{V_p} + \frac{V_{go}^2}{V_p^2} + \tfrac{1}{2}\frac{V_{g1}^2}{V_p^2}\right] \quad . \tag{15}$$

Note that $V_o = V_{bias}$ of Figure 1.

Also,

$$I_1 = 2I_{dss}\left(1 - \frac{V_{go}}{V_p}\right)\frac{V_{g1}}{V_p} \qquad J_1 = 0 \tag{16}$$

$$V_1 = -2\,\frac{(V_b - V_T)}{(1 + \phi/V_p)^2}\,\frac{V_{g1}}{V_p}\left(1 - \frac{V_{go}}{V_p}\right) \qquad U_1 = 0. \tag{17}$$

Equations (3) and (4) can be manipulated to yield

$$\frac{V_{go}}{V_p} = \frac{(1 - \phi/V_p)}{2} \tag{18}$$

$$\frac{V_{g1}}{V_p} = \frac{(1 + \phi/V_p)}{2} = \left(1 - \frac{V_{go}}{V_p}\right) \quad . \tag{19}$$

Using Equations (18) and (19), Equations (14) through (17) can be expressed as

$$I_o = \tfrac{3}{2}\, I_{dss}\left(\frac{1 + \phi/V_p}{2}\right)^2 \tag{20}$$

$$V_o = V_b - \tfrac{3}{8}\,(V_b - V_T) \tag{21}$$

$$I_1 = 2I_{dss}\left(\frac{1 + \phi/V_p}{2}\right)^2 \tag{22}$$

$$V_1 = -\tfrac{1}{2}(V_b - V_T) \quad . \tag{23}$$

From Equations (10), (20), and (21) the dc input power is found to be

$$P_{dc} = \tfrac{3}{8} I_{dss}(1 + \phi/V_p)^2 \left[V_b - \tfrac{3}{8}(V_b - V_T)\right] \quad . \tag{24}$$

The fundamental rf power is

$$P^1_{rf} = \tfrac{1}{8}(V_b - V_T)\, I_{dss}(1 + \phi/V_p)^2 \quad . \tag{25}$$

The drain efficiency for Class A operation becomes

$$\eta^1_A = \frac{P^1_{rf}}{P_{dc}} = \frac{1}{3}\,\frac{(V_b - V_T)}{(V_b - \frac{3}{8}V_b + \frac{3}{8}V_T)} \quad . \tag{26}$$

For Class B operation Equations (3a), (3b), and (4) become

$$V_{go} = V_p \tag{27}$$

and

$$V_{g1} = V_p + \phi \tag{28}$$

$$V_{b_{max}} = V_B - 2V_p - \phi \quad . \tag{29}$$

A pictorial representation of Class B operation is shown in Figure 2. The output current and voltage waveforms can be expressed by the following equations:

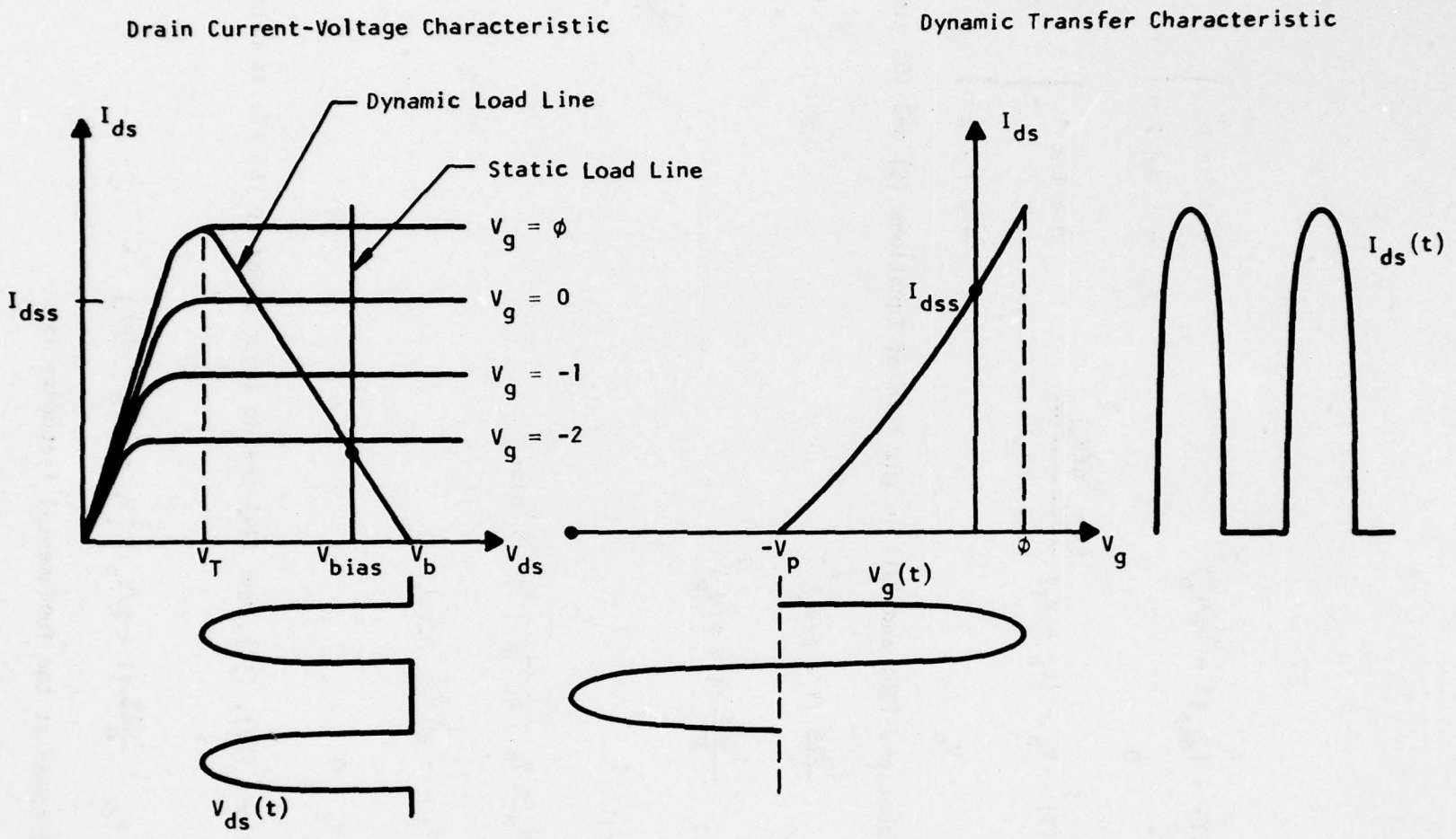


Figure 2 FET Common Source Characteristics (Class B)

$$I(T) = I_{dss}(1 + V_g/V_p)^2 \qquad 0 \le T \le \pi$$
$$= 0 \qquad \pi < T \le 2\pi \qquad (30)$$

$$V(T) = V_b - (V_b - V_T)\frac{(1 + V_g/V_p)^2}{(1 + \phi/V_p)^2} \qquad 0 \le T \le \pi$$
$$= V_b \qquad \pi \le T \le 2\pi \qquad (31)$$

Expanding Equations (30) and (31) in the form of Equations (5) and (6) yields

$$I_o = \frac{I_{dss}}{4}(1 + \phi/V_p)^2 \qquad (32)$$

$$I_1 = \frac{4I_{dss}}{3\pi}(1 + \phi/V_p)^2 \qquad (33)$$

$$J_1 = 0$$

$$V_o = V_b - \frac{1}{4}(V_b - V_T) = V_{bias} \qquad (34)$$

$$V_1 = -\frac{4}{3\pi}(V_b - V_T) \qquad (35)$$

$$U_1 = 0 \quad .$$

From Equations (10), (32), and (34) the dc input power to the FET is determined to be

$$P_{dc} = \frac{I_{dss}}{4}(1 + \phi/V_p)^2\left[V_b - \frac{1}{4}(V_b - V_T)\right] \quad , \qquad (36)$$

and the rf power at the fundamental frequency is

$$P_{rf}^{1} = \frac{8}{9\pi^2} (V_b - V_T)\, I_{dss}(1 + \phi/V_p)^2 \quad . \tag{37}$$

The drain efficiency is expressed by

$$\eta_B^1 = \frac{32}{9\pi^2} \frac{(V_b - V_T)}{[V_b - \frac{1}{4}(V_b - V_T)]} \quad . \tag{38}$$

Using Equations (25) and (26) for Class A operation and Equations (37) and (38) for Class B operation, the output powers and drain efficiencies for operation into a resistive load were calculated. For comparison, similar calculations were made for the case of a linear dynamic transfer characteristic. The basic approach is the same as detailed above for the square law characteristic.

The best means for comparing results for different modes of operation is to compute the maximum theoretical efficiency. This has been done for the cases mentioned above, and the results are given in Table 1. Also included in the table are the results for a square wave input. In this case the shape of the dynamic transfer characteristic does not affect the results of the calculation, nor does the input bias level. Finally, the results for a tuned power amplifier are included in the table. These calculations, which were originally made for electron tubes, are available in the literature[1] and are not repeated here. It is noted that for a square law characteristic and Class B operation into a tuned load the theoretical maximum efficiency is 85%. It can be shown (using the dc and fundamental components of the resultant output current waveform) that for this case the expression for the maximum possible drain efficiency reduces to one-half the ratio of the amplitude of the fundamental component of current to the dc or average component of current. The assumptions used are similar to the ones made in the literature concerning Class B operation into a tuned load with a device having a linear transfer characteristic.

Table 1

Maximum Amplifier Efficiencies

Amplifier Class	Transfer Characteristic	Load	Efficiency*
A	Linear	Resistive	50
A	Square law	Resistive	53
A or B (square wave input)	Either	Resistive	81
B	Linear	Resistive	58
B	Square law	Resistive	48
B	Linear	Tuned (zero impedance at harmonics)	79
B	Square law	Tuned (zero impedance at harmonics)	85

*Drain efficiency

Namely, it is assumed that the only voltage developed across the load resistor is that at the fundamental frequency, and that the peak value of this voltage waveform equals the dc drain bias voltage.

The efficiency calculations presented in Table 1 indicate that Class B operation of an IGFET amplifier into a tuned load (zero impedance at harmonic frequencies) is the most promising approach to high efficiency operation. An alternative approach would be to use a square wave input signal; however, this approach would require wave shaping at the input to the amplifier.

As a preliminary test of the theoretical analysis, a number of conventional GaAs MESFETs were tested as X-band amplifiers to determine the bias conditions which gave maximum output power and efficiency. The maximum power was observed at low gate bias, and maximum efficiency was obtained with gate bias approaching the pinchoff voltage (V_p), i.e., approaching Class B operation. Equations (25) and (37) can be manipulated to yield the expected power reduction for Class B operation. The maximum power achievable under Class B operation is seen to be 72% of the maximum power under Class A operation. A typical three-cell device having V_p = 3.5 V has a maximum output power of 950 mW at 8 GHz with 4 dB gain when V_g = -0.6 V. The drain efficiency was measured at 59.8%, indicating some squaring of the input waveform and probably some harmonic tuning in the output circuit. With V_g = -3.0 V the output power of the device drops to 740 mW with 4 dB gain, while the efficiency increases to 81.4%. Again, the high value of measured efficiency indicates favorable distortion of the input waveform or harmonic tuning in the output circuit, or, more likely, some degree of both. The 22% reduction in power falls within the theoretical prediction. When V_g is increased to -3.5 V (true Class B bias condition), the efficiency remains at 81.4%, but the output power decreases to 690 mW (a 27.4% reduction) with 4 dB gain.

Thus, maximum efficiency is expected for operation under Class B conditions, provided that the ratio of the gate breakdown voltage to the pinchoff voltage can be increased significantly. The potential means of achieving the desired ratio improvement exists in the form of an FET with an insulated or semi-insulated gate.

SECTION III
GaAs IGFETS

The GaAs IGFET device is a field effect transitor in which the gate metal is separated from the GaAs channel by a thin layer of insulating material. The presence of the insulating material prevents the flow of charge between the gate metal and channel as is possible through the depletion layer in the conventional FET structure. Hence, a "forward" voltage applied to the gate of an IGFET will result in an accumulation of electrons at the channel-insulator interface with consequent conductivity modulation of the channel. A large dc "reverse" voltage can generate an inversion layer of charge at the insulator-channel interface if adequate time is allowed for its generation. However, deep depletion of the channel charge and its accompanying conductance modulation of the channel still occur, similar to the action in a conventional FET structure. The increased gate voltage span offered by the IGFET structure because of these fundamental charge transport limitations makes it particularly interesting when operated as a Class B amplifier where high gate voltage amplitudes are encountered.

The major problem with the device is obtaining an insulating layer that allows the benefits outlined above. It is essential to obtain pure layers that contain no mobile (mostly ionic) charge and that have a low surface state density at the interface with the GaAs channel. With silicon devices such high quality insulators and interfaces can be provided by oxide films.

To examine anodically formed oxide films as possible insulators for GaAs IGFETs, a series of slices was subjected to oxidation using a tartaric acid-propylene glycol electrolyte. This electrolyte has been reported[2] to yield oxide films with very low surface state densities and superior dielectric properties. The slices were oxidized at different voltages to provide a range of oxide thicknesses, and half of each slice was later annealed for 6 hours at 300°C in hydrogen. No change in appearance was noted as a result of the anneal; however, for the thinner films the ellipsometrically determined refractive index increased slightly. To ascertain the surface state densities, MOS

structures were formed on the anodically oxidized surfaces by patterning Al dots that were subsequently subjected to capacitance-voltage and conductance-voltage measurements. The conductance and capacitance data were obtained by measuring, respectively, the phase-locked and quadrature-phase components of the current response to a 10 mV signal voltage applied across the sample. The frequency of the ac signal could be varied between 1 Hz and 100 kHz and was impressed on a dc ramp voltage that was swept between preset voltage limits at an adjustable rate. In addition, C-V data were obtained at 1 MHz with a Boonton capacitance meter. A typical data set is shown in Figure 3. In each case the curves of Figure 3 were obtained by sweeping from deep depletion (-9 V) toward accumulation. Note that the G/ω data show a broad peak near zero voltage indicative of a relatively uniform density of states near mid-gap. Accurate analysis of the data was complicated by the nonideal characteristics of the oxides. However, by adopting a simple surface state model, one obtains a surface state density between 7.9 and 14×10^{11} cm^{-2} eV^{-1} near mid-gap. It can be concluded that the films show relatively low surface state densities for anodically grown oxides. However, the values are higher than those of thermal oxides on Si, which have benefited from extensive development efforts.

A large frequency dispersion of the accumulation capacitance was observed. It has been suggested that the source of the dispersion is the Maxwell-Wagner effect due to a metamorphic layer between the oxide and the GaAs. If so, one might expect the dispersion to reappear in heavy inversion; however, it does not. The conductance data indicate another possibility, which is an increasing density of surface states near the band edge. Further work to investigate this possibility will require oxides that can sustain higher voltage without excessive leakage and reduction of the hysteresis loop. Both of these effects are indicative of charge states in the oxide that affect MOS properties as much as interface states.

In an effort to improve the insulating characteristics of GaAs anodic oxides, two new series of slices were prepared. One series consisted of oxides that were grown at significantly lower current densities (< 1 mA/cm^2), while the slices from

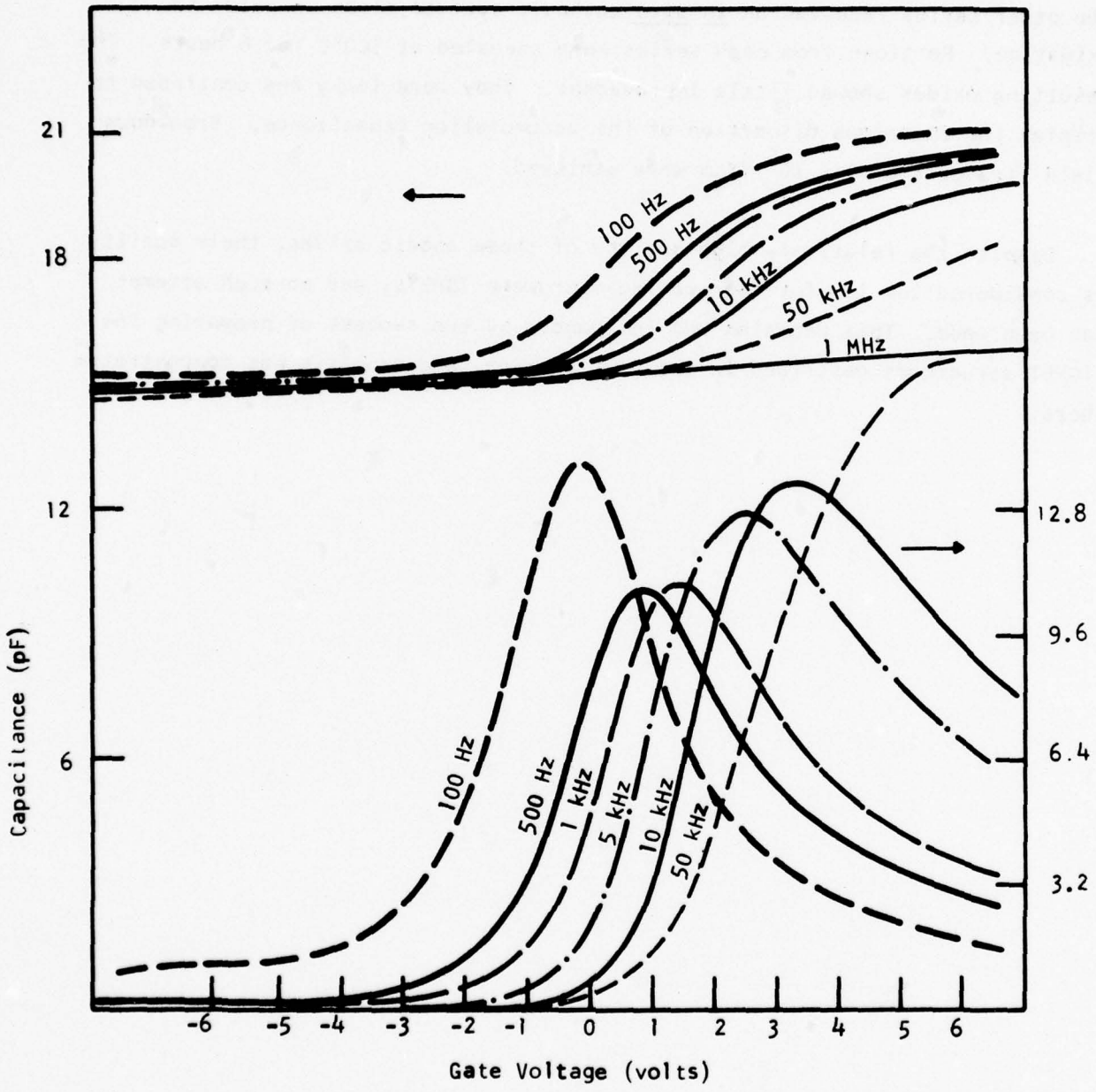


Figure 3 C - V and G/ω - V Curves Obtained from MOS Capacitors Incorporating an Anodically Grown Oxide at Various Frequencies as Labeled

the other series received an *in situ* cathodic surface clean-up prior to oxidation. Portions from each series were annealed at 300°C for 6 hours. The resulting oxides showed little improvement. They were leaky and continued to display the anomalous dispersion of the accumulation capacitance. Breakdown field strengths of 3×10^6 V/cm were achieved.

Despite the relatively high quality of these anodic oxides, their quality is considered too low for fabricating microwave IGFETs, and no such attempt has been made. This decision was influenced by the success of preparing the SIGFET structures described in the next section, and emphasis was concentrated there.

SECTION IV
GaAs SIGFETS

The GaAs SIGFET is similar to a conventional FET, but with the important modification of including a thin semi-insulating layer of GaAs under the gate metal. The semi-insulating layer is usually an intimate part of the depletion under the gate metal, but it can transport charge either in avalanche or in forward bias injection. Of course, it significantly increases the breakdown voltage, and the forward voltage drop can be high because of the series resistance of the semi-insulating layer. From the standpoint of use in a Class B amplifier, the extended voltage range of the SIGFET gives it similar advantages to the IGFET. Practically, the SIGFET can be fabricated by ion-bombarding the surface or by epitaxial growth. In either case, the problems associated with the channel interface are minimized relative to the IGFET. Details of the SIGFET device are considered in this section.

The basic structure and device physics of the conventional GaAs MESFET are reviewed first, followed by a discussion of the reasons for developing the SIGFET. The next subsection describes the fabrication process for the GaAs SIGFET and optimization of the ion-bombardment conditions. Then the dc and rf characteristics of the GaAs SIGFETs are presented and compared with those of companion GaAs MESFETs.

A. Device Principles

Consider the simplified sketch of the basic GaAs FET device structure shown in Figure 4. An n-type layer of uniform shallow donor doping N_d and thickness a is grown epitaxially on an insulating substrate. Ohmic source and drain contacts of width Z are placed as shown. Between them is a Schottky barrier "gate" of length ℓ. In normal operation the source is grounded and a positive voltage $+ V_{ds}$ is applied to the drain, causing current I_{ds} to flow from drain to source under the gate. The n-type GaAs under the gate is depleted of carriers in the Schottky barrier space-charge region, with a negative gate voltage V_g increasing the depletion depth. Thus, changes in gate voltage modulate the drain

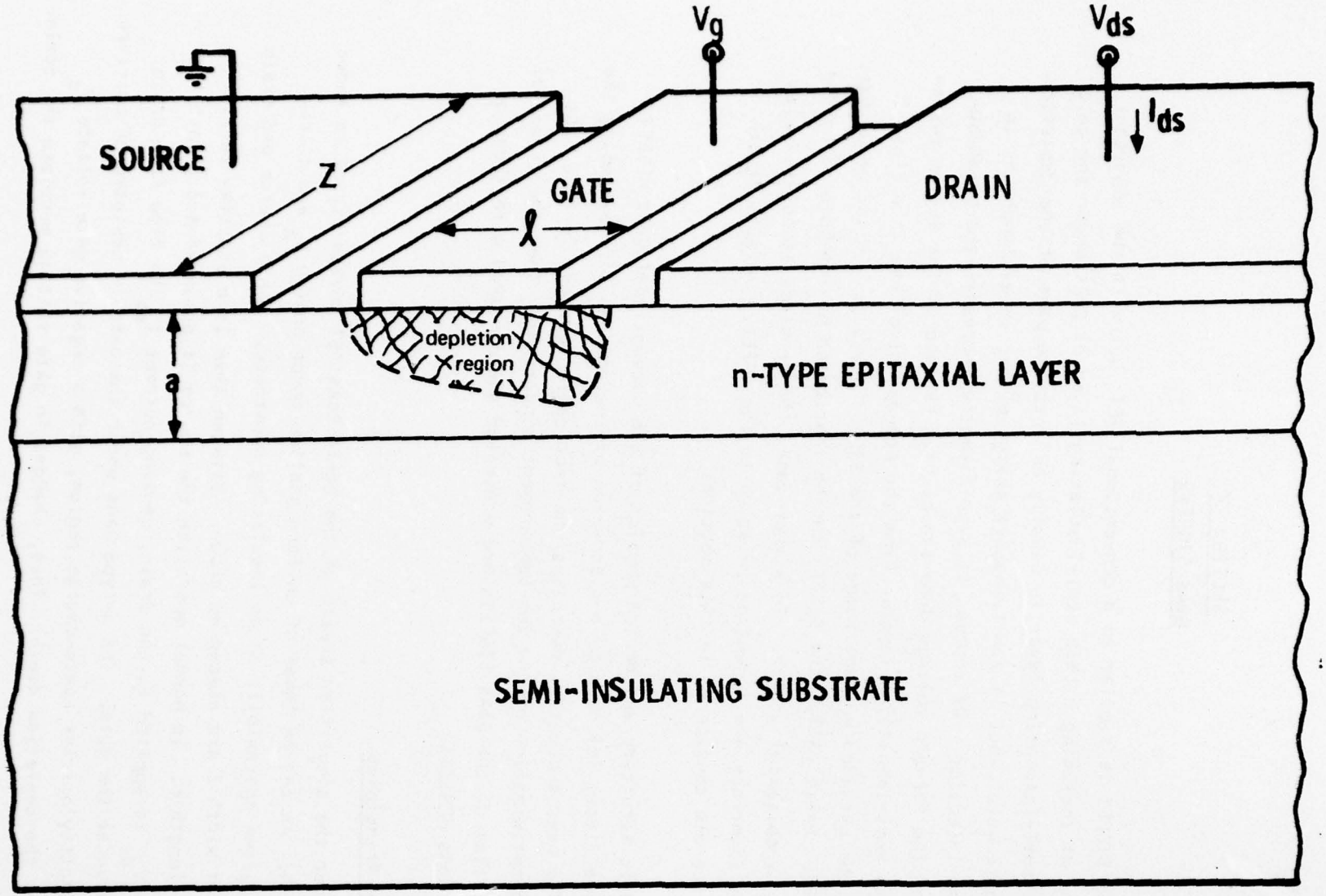


Figure 4 Simplified Sketch of the Basic GaAs MESFET Device Structure

current I_{ds}. If V_g is large enough, the depletion region of the gate reaches the insulating substrate, and conduction is entirely "pinched off" ($|V_g| \equiv V_p$). If the epitaxial thickness is large, the gate Schottky barrier may break down before pinch-off can occur.

As V_{ds} increases with $V_g = 0$, I_{ds} increases linearly at first, and then saturates at a current I_{dss} beginning at a threshold voltage V_T. This saturation is caused by the forward drain bias effectively reverse-biasing the gate and pinching off the conducting channel. Also contributing to current saturation is the fact that at higher drain voltages electron velocity in saturation occurs. The saturation current decreases as V_g is made more negative. In actual operation, the dc values of V_{ds} and V_g are fixed such that the device is biased into saturation, an rf signal is applied between the gate and source, and an amplified signal is available across the drain and source. Device output power increases at higher drain voltages, but at large drain bias the large negative bias of the gate with respect to the drain causes the gate Schottky barrier to avalanche. This occurs first during the negative portion of the rf input waveform and causes the device output power to stop increasing. The larger Joule heating of the device at higher drain voltages also reduces output power.

The incorporation of a semi-insulated gate region into a GaAs FET structure was first reported by Pruniaux, North, and Payer,[3] who implanted protons across the entire source-drain gap to create a semi-insulating layer beneath the gate. They proposed that the semi-insulating layer would permit the use of higher epitaxial doping levels (and hence higher device transconductance and better performance) without the problem of gate breakdown. In addition, the device could be operated with a gate bias of either polarity. However, as discussed earlier, the extended voltage range resulting from the use of a semi-insulated gate region is desirable for Class B amplifier operation. In the present work,

in order to properly evaluate the effect of the semi-insulated gate region on power FET operation, both conventional MESFETs and SIGFETs were fabricated from the same epitaxial material.

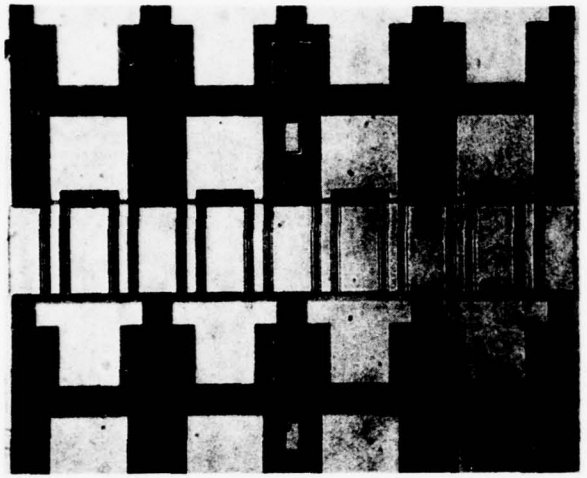
B. Device Fabrication

The fabrication process for GaAs SIGFETs is very similar to that for GaAs MESFETs so the latter is described below. The process changes for the SIGFET are then enumerated.

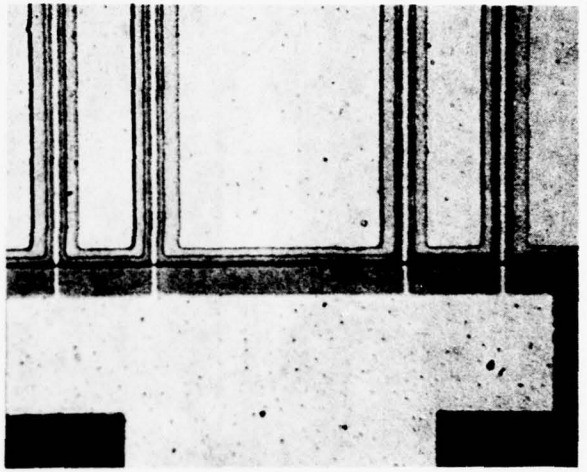
The GaAs power devices have 2 μm gate lengths, 6 μm source-drain spacings, and are made up of four cells, each with 600 μm gate width. The total gate width can therefore be varied from 600 μm to 2400 μm, depending on the number of cells that are connected. Photographs of a device taken during the fabrication procedure are shown in Figure 5. The active GaAs layer is grown by vapor phase epitaxy on a semi-insulating Cr-doped GaAs substrate. The doping level of the active region is $\sim 1 \times 10^{17}$ cm^{-3}, and the layer thickness has been reduced by the anodic etching technique to a uniform thickness of ~ 0.3 μm.

The basic process is quite simple, with only three major device processing steps,[4] as illustrated in Figure 6. Following epitaxial thinning, the first major processing step is to etch mesas through the thin n-layer to the semi-insulating substrate. This isolates the source and drain terminals except for the channel under the gate and provides an insulated surface for the gate bonding pad. A mesa height of 0.5 to 1.0 μm is adequate to isolate adjacent mesas (resistances of 1 to 10 MΩ).

The second step is the source/drain metallization. A lift-off pattern is defined in AZ-1350 photoresist and the source/drain metal is evaporated over the slice. The unwanted metal is lifted off by dissolving the photoresist in acetone. This method of metal definition is very simple, gives sharp edge definition, and is capable of extremely fine geometries. The metal remaining on the source and

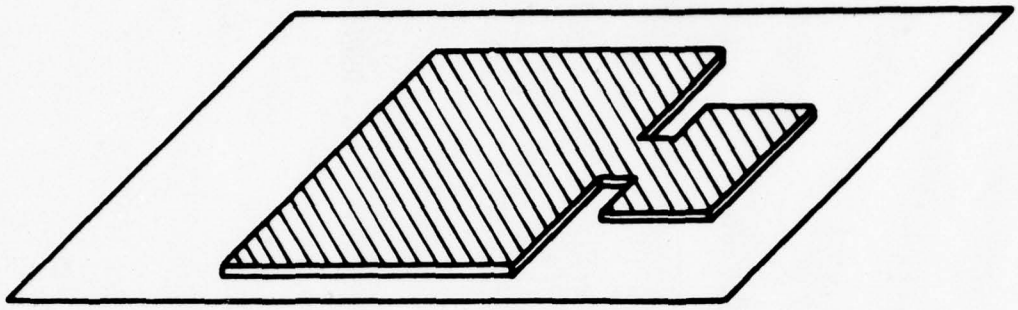


Overview

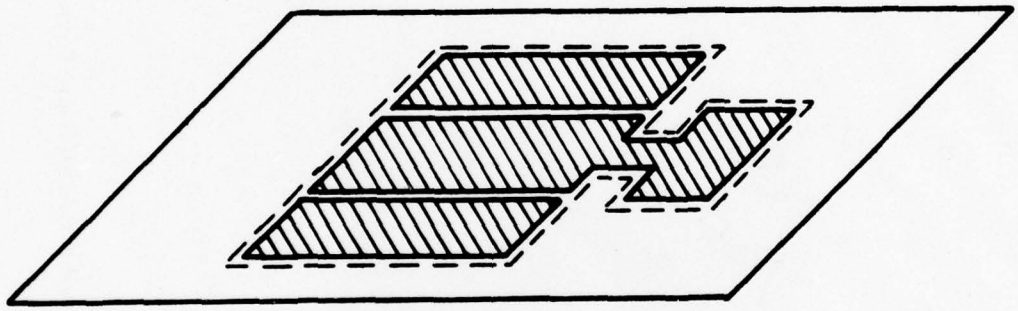


Gate Region

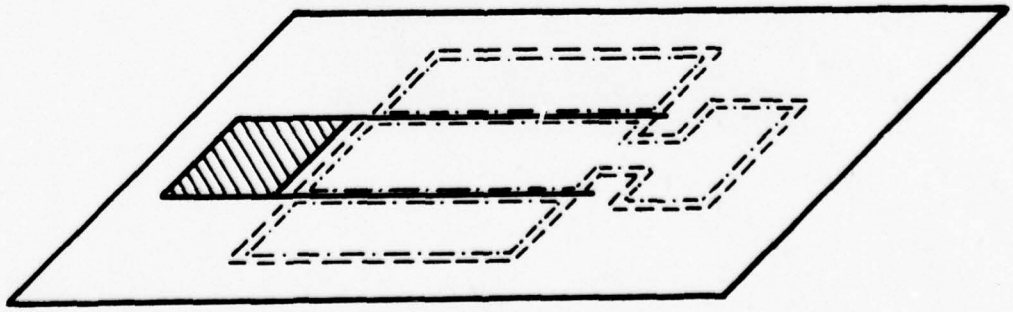
Figure 5 Photographs of 2400 μm Gate Width GaAs Power FET



MESA ETCH



SOURCE AND DRAIN METALLIZATION



GATE METALLIZATION

Figure 6 Planar Device Fabrication Process

drain is then alloyed into the GaAs, forming an ohmic contact. After studying several alloys for use as an ohmic contact, AuGe with a thin Ni overlay was chosen because of its low contact resistance. The ohmic contacts are formed by evaporating approximately 2000 Å of eutectic composition AuGe followed by a 200 to 400 Å Ni overcoat. Alloying is accomplished by raising the slice to 450°C for several seconds in flowing helium.

The third major processing step is the gate metallization. The gate pattern is defined in photoresist, and the metal is evaporated and lifted off as with the source and drain. The alignment of the gate in the source-to-drain gap is the most critical step. To recess the gate, a groove is etched in the GaAs surface after the gate pattern is defined, immediately prior to gate metal evaporation. The recess depths achieved have been in the range 500 to 2500 Å, which can lead to as much as 50% reduction in the parasitic resistance.

Aluminum is used as the gate metal. It has been shown to be less subject to degradation with time at elevated temperatures than other gate metallizations that have been used. Evaporation is carried out at about 50°C with a glow-discharge prior to deposition to ensure good adhesion.

Following the gate metallization, a layer of Cr/Au is evaporated on the source and drain bonding pads to improve current spreading and bondability. A nitride layer is then deposited in the active region, and a thick (10 to 15 μm) Au layer is plated to the source pads to simplify bonding.

The source pads are 0.003 inch wide, near the minimum size for stitch bond interconnection. This leads to a total chip width of 0.040 inch (to accommodate 2400 μm total gate width), which is not too large for X-band operation. The chip thickness is approximately 0.004 inch. An SEM photograph of a bonded device is shown in Figure 7.

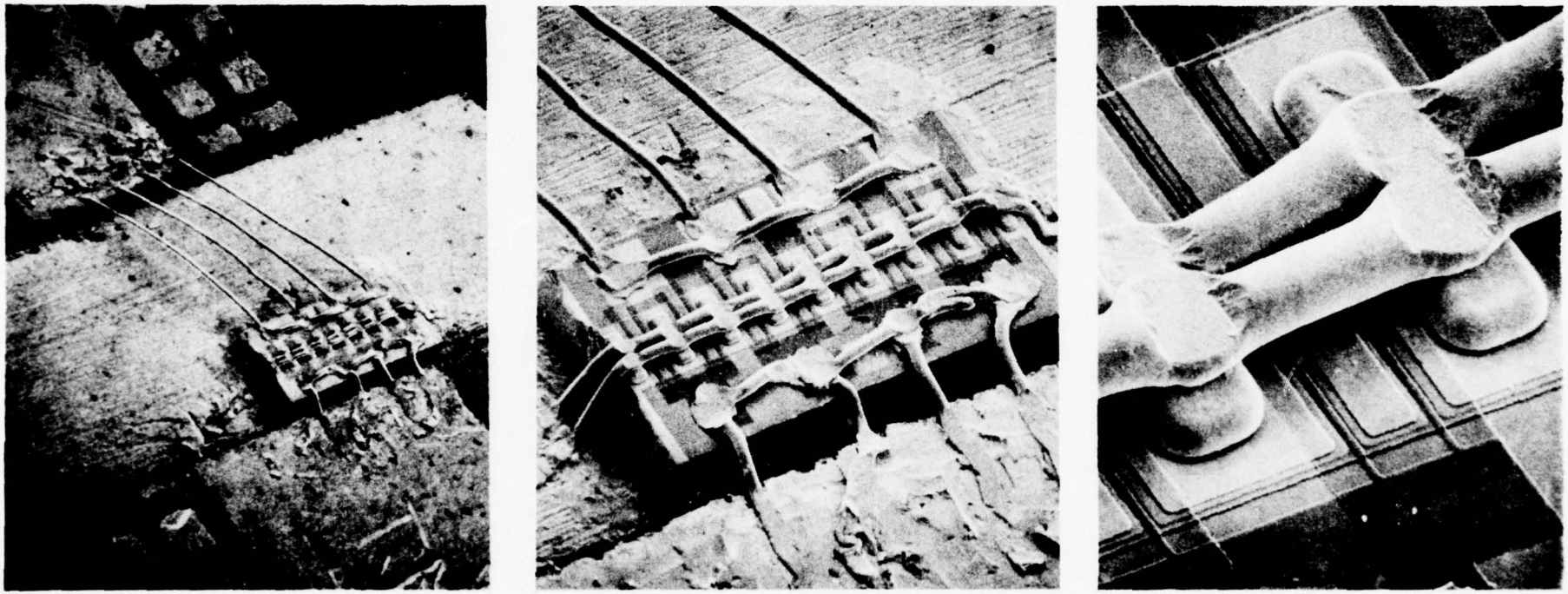


Figure 7 Scanning Electron Micrographs of 2400 μm Gate Width GaAs FET Mounted on a Cu Block

Pruniaux, et al., fabricated semi-insulated gate devices by bombarding the entire active region with protons. However, for material with optimum epitaxial thickness, it was discovered that protons accelerated to minimum energy available with our implantation equipment (30 keV) penetrated the entire active region, reducing the channel conductivity to zero. This problem was solved by bombardment with heavier ions (Ar) to reduce the penetration depth commensurate with the thinner epitaxial layers of modern devices. Initially, the slices were implanted across the entire surface after the source and drain contacts had been applied. These devices had poor dc and rf performance characterized by low transconductance, light-sensitive I-V characteristics, high leakage current, and low gain. As a result, the process was modified to confine the bombardment region to the area immediately below the gate metallization. The gate pattern is defined in photoresist as with the conventional MESFET, but rather than evaporating the gate metal, the slice is bombarded with Ar^+ ions. The gate metal is then evaporated and the process continued. This results in a device having a semi-insulating region localized just beneath the gate metal as shown in Figure 8. As discussed in detail below, the optimum parameters were found to be 10^{14} Ar^+ ions/cm^2 at 30 keV. The thick unimplanted source-gate and drain-gate regions provide the same parasitic resistance reduction that the gate recess does for conventional MESFETs. Since the implantation process neither degrades nor penetrates the photoresist, the gate metal evaporation and lift-off can take place following implantation with no additional processing steps.

The effective depth of different implant energies and fluxes was determined by measuring the source-drain saturation current (with no gates present) before and after implantation. This information, combined with the epitaxial layer resistivity, allows the effective implant depth to be calculated. The results for a slice cleaved into several pieces which were subjected to 10^{14} Ar^+ ions/cm^2 at different energies are summarized in Table 2.

In a similar experiment several pieces from a slice were subjected to different dosages of 30 keV Ar^+ ions. The resulting effective implant depths are summarized in Table 3. As will be described later, measurements on devices

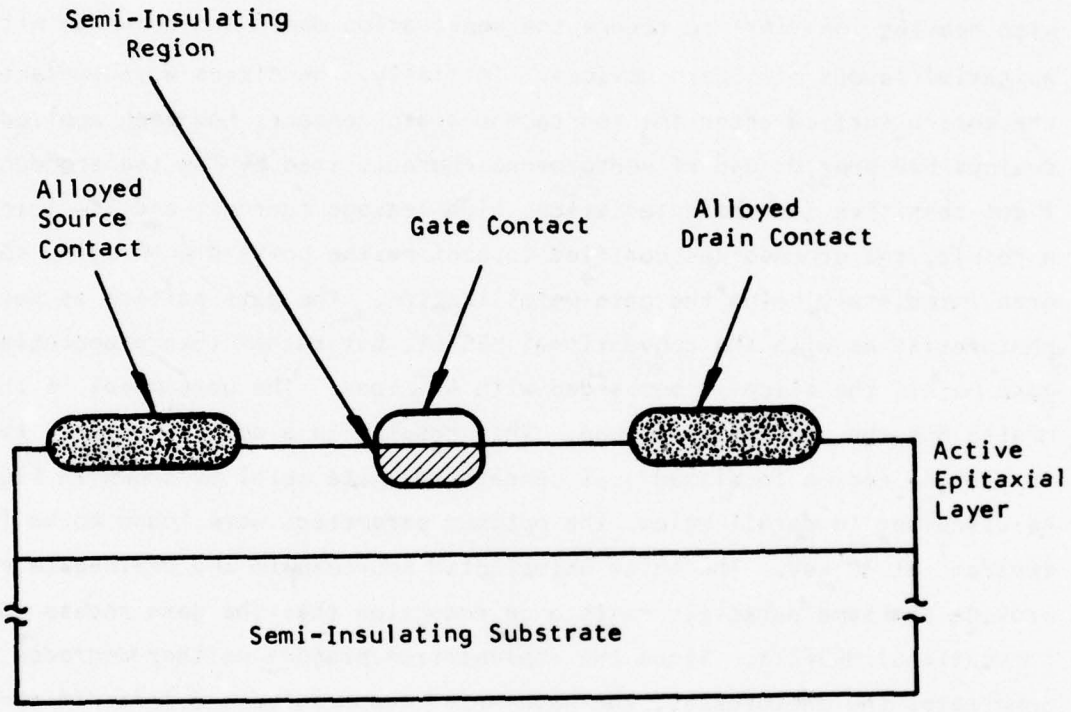


Figure 8 Basic SIGFET Structure

Table 2

Effective Implant Depth as a Function of Energy for 10^{14} Ar^+ Ions/cm^2

$10^{14}/cm^2$ Ar^+ Implant Energy (keV)	Effective Depth (μm)
30	0.21
60	0.43
120	0.55
200	0.80

Table 3

Effective Implant Depth as a Function of Implant Dose for 30 keV Ar^+ Ions

30 keV Ar^+ Implant Dosage (per cm^2)	Effective Depth (μm)
10^{12}	0.08
10^{13}	0.17
10^{14}	0.21
10^{15}	0.29

fabricated from these slices indicated that the optimum Ar^+ bombardment conditions were an accelerating voltage of 30 keV and a dosage of 1×10^{14} cm^{-2}. An alternate approach was examined in which the entire active area was implanted with Xe^+ (30 keV, 10^{14} cm^{-2}). This was followed by the customary (and deeper) Ar^+ implant just under the gate, giving the structure of Figure 9(b). The resulting devices had high gate leakage currents and low gains, just as did the channel-wide implanted devices [Figure 9(a)] discussed earlier. Apparently, for optimum SIGFET performance the implanted region must be confined to the area just beneath the gate metal.

SIGFETs were also fabricated from slices in which the semi-insulating region was not produced by ion bombardment, but by the epitaxial growth of a high resistivity, undoped layer on top of the normally doped active layer. These devices, which are called "epitaxial SIGFETs" to distinguish them from SIGFETs produced by ion implantation, have three sequentially grown layers: a buffer layer, an active n layer, and a semi-insulating layer. Before device fabrication begins, a C-V doping profile is obtained to determine the thickness of the semi-insulating layer. A typical profile is given in Figure 10. Device fabrication then proceeds as described above, except that the ohmic source/drain contacts are achieved by etching to recess the source/drain regions below the high resistivity surface layer prior to metallization, lift-off, and alloy. The amount of recess required is estimated from knowledge of the semi-insulating layer thickness obtained from the C-V doping profile. This has proved to be a viable procedure for achieving source/drain contacts through the semi-insulating layer. If this layer is too thick for optimum performance, it is necessary to etch it as well, thus recessing the gates. Of course, care is taken to prevent this recess from extending completely through the semi-insulating region.

C. Dc Characteristics

The I-V characteristics of SIGFET devices are significantly different from those of MESFETs fabricated from the same slice.[5] The most pronounced change

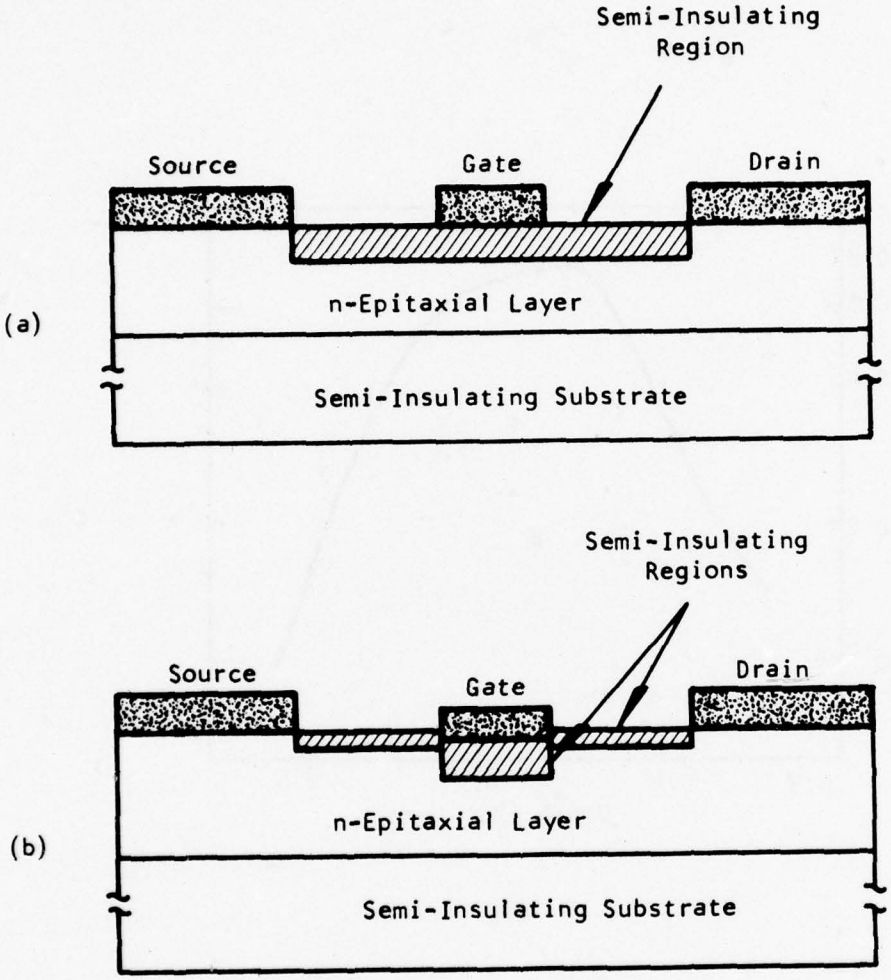


Figure 9 Variations on the SIGFET Structure. (a) Channel-wide implant (b) Two-level implant

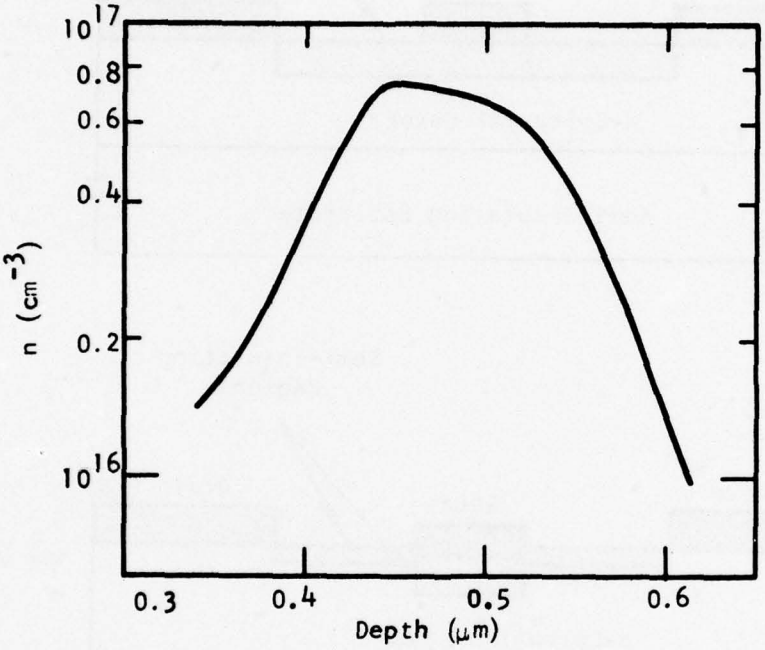


Figure 10 C-V Doping Profile of an Epitaxial SIGFET

is a much larger gate breakdown voltage for the SIGFET. Figure 11 shows the gate-drain I-V characteristics of a SIGFET device and a companion MESFET fabricated from the same slice. Both devices have gate-drain current of about 0.05 μA at 5 V; however, the MESFET gate breaks down at a reverse voltage of approximately 12 V, while the SIGFET breaks down at 25 to 30 V, which is more typical of bulk material having a carrier concentration of 5 to 6 x 10^{16}. This increase is probably due to a change in the electric field profile beneath the implanted region that eliminates breakdown-causing high field regions near the metallization edges. Figure 11 also shows the somewhat higher forward bias could be applied to the SIGFET, as indicated by Pruniaux, et al.,[3] but the effect on device microwave performance is probably small. Figure 12 shows the drain characteristics for these two devices. One noticeable difference is that the SIGFET has about 20% lower maximum transconductance.

The saturation current, source-drain burnout voltage, and reverse gate breakdown voltage were also evaluated as a function of the applied implant energy and dose used to produce the SIGFETs. The more meaningful comparisons, of course, are those in which devices with different implant parameters originate from the same slice and are processed simultaneously. This tends to reduce variations in performance that could be attributable to differing slice characteristics or processing procedures. The following implant energies and doses were used for this comparison:

Slice	Flux (cm^{-2})	Ar^+ Implant Energy (keV)
A	10^{14}	30, 60, 120
	10^{15}	30
B	10^{14}	30
C	10^{13}	30

The test data are presented in Figure 13. The three dc tests will be discussed separately with reference to Figure 13.

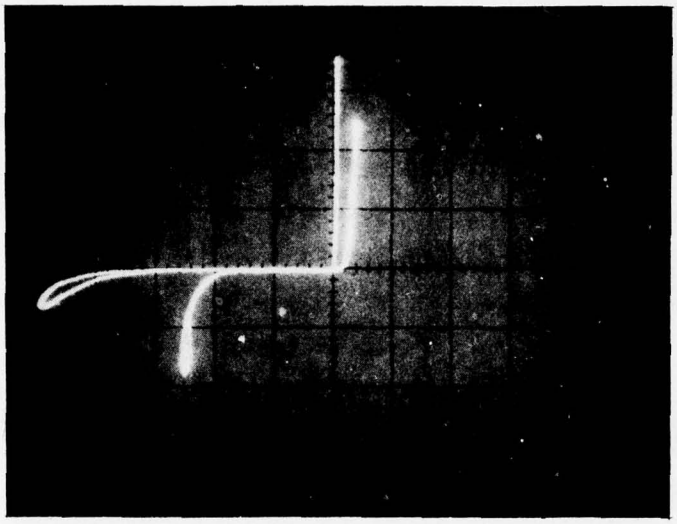
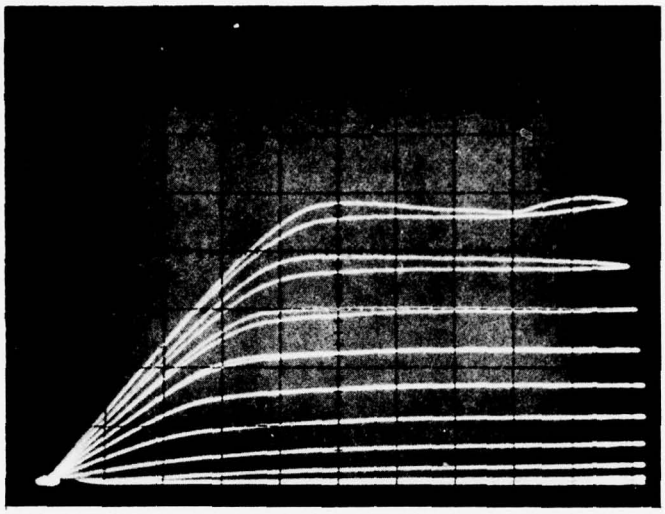
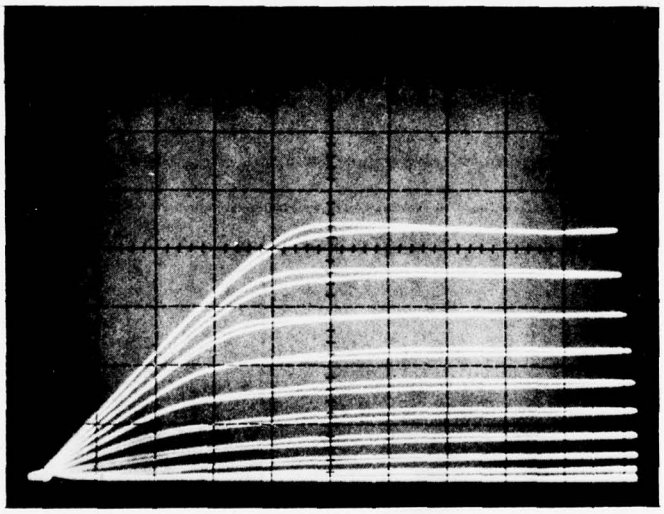


Figure 11 Gate-Drain Current-Voltage Characteristics of SIGFET and MESFET Devices Fabricated from the Same Slice. 100 μA/vertical division, 5 V/horizontal division.



(a) MESFET



(b) SIGFET

Figure 12 Comparison of Drain Characteristics of 300 μm Gate Width SIGFET and MESFET Devices Fabricated from the Same Slice. Both photographs have 20 mA/vertical division, 0.5 V/horizontal division, 1 V/step.

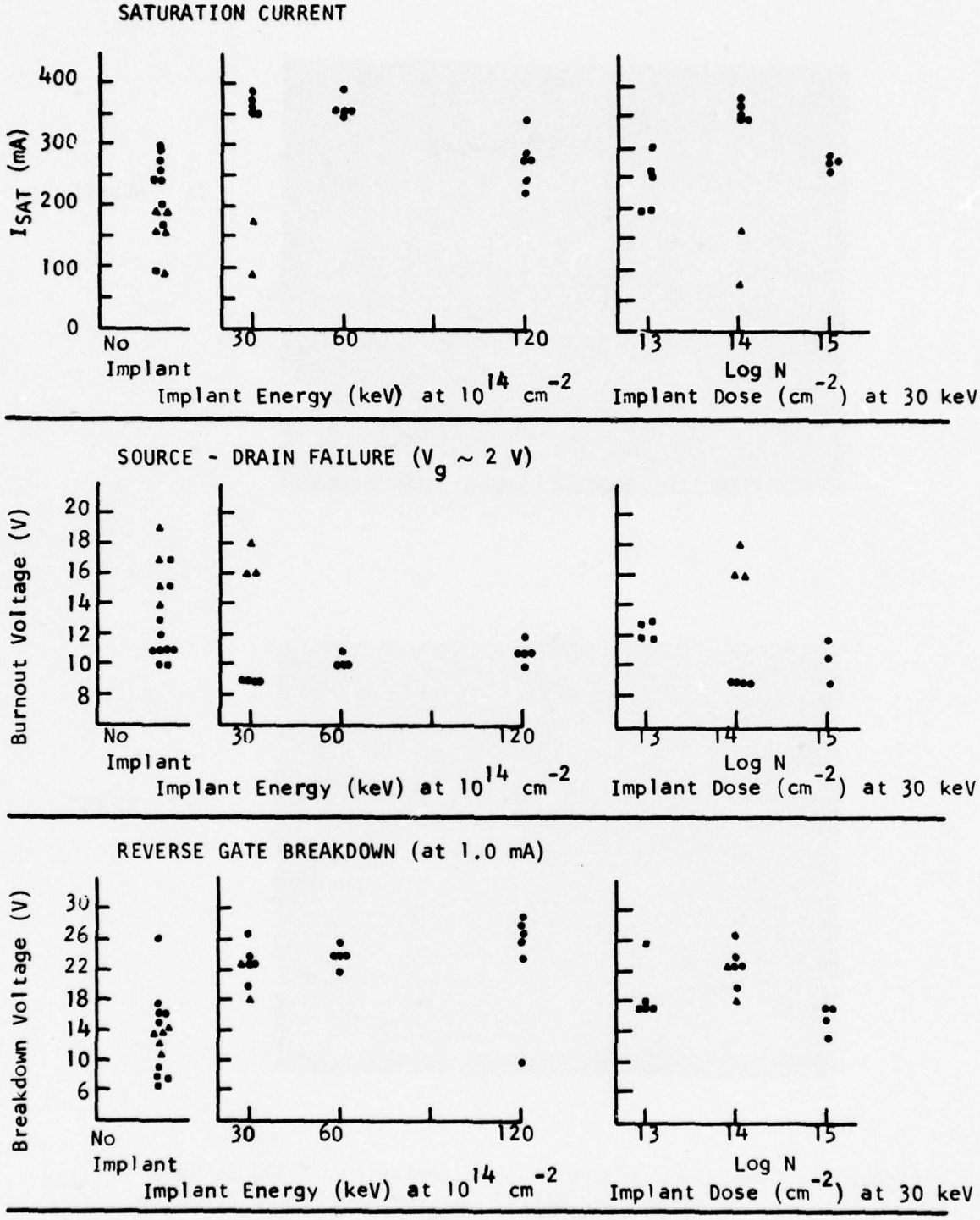


Figure 13 Dc Characteristics of SIGFET Devices as a Function of Ar^+ Implant Energy and Dose

1. Saturation Current

The figure indicates only moderate variations of saturation current in a given slice for various implant energies and doses. This result, however, was purposely produced during fabrication. A slice that had been anodically thinned to completion, and hence was of nearly uniform thickness, would have exhibited larger variations in I_{SAT} for different implant energies and doses due to the corresponding variations in the effective depth of the semi-insulating region. However, for the comparisons to be made in this experiment, it was desired to produce devices with reasonably equivalent saturation currents. This was done by anodically thinning each slice only until it just began to "clear." This resulted in a slice slightly thicker than normal that still had thickness variations. The thicker regions were then used for the greater implant energies or doses. In the case of the unimplanted portions, gate recess was used to adjust the saturation current.

2. Source-Drain Failure Voltage

For this test, a bias of - 2 V was applied to the gate, and the source-drain bias was slowly increased until failure occurred. No microwave signal was present. The failures resulted in a short between source and drain. Referring to Figure 13, there is little difference in source-drain burnout voltage for different implant conditions in devices originating from the same slice. The moderate variation that is present correlates inversely with the saturation current (see data for slice A, Figure 13). Hence, it is likely that the slight increase (decrease) in I_{SAT} is causing the slight decrease (increase) in burnout voltage. Again, the relevant point is that there is no critical dependence on implant conditions within the range tested.

3. Reverse Gate Breakdown Voltage

This test was performed by reverse-biasing the gate with respect to the source and noting the voltage required to draw 1.0 mA of reverse gate current. As indicated by the data in the figure, the reverse gate breakdown

voltage is increased by approximately 8 V upon implantation of 10^{14} cm^{-2} 30 keV Ar^+. Only minimal additional improvement is observed when the same dose is implanted at 120 keV. An increase of the 30 keV dosage to 10^{15} cm^{-2} seems to result in no improvement.

It concluded from these experiments that at doses of 10^{14} cm^{-2}, implantation results in higher reverse gate breakdown voltages and that this improvement is not critically dependent on implant energy in the range tested. This high reverse gate breakdown voltage is the principal distinguishing characteristic of a SIGFET.

Epitaxial SIGFETs were also subjected to the same dc characterization tests just described. Although there were no control slices with which to make direct comparisons, the device characteristics were found to be essentially the same as those of SIGFETs produced by 10^{14} cm^{-2} 30 keV Ar^+ ion implantation. Saturation current and pinch-off voltage varied more in the epitaxial SIGFETs because the self-limiting anodic oxidation process could not be used in their fabrication.

D. Rf Characteristics

1. Cw Operation

The microwave performance of GaAs SIGFETs was measured at X-band and compared with that of companion MESFETs fabricated on the same slice. Typically, the gain with 5 V drain bias and 15 dBm input power was measured. The maximum output power with 4 dB gain at 8 V drain bias and the highest output power achievable with 4 dB gain at any drain bias were also measured. In general, the conventional MESFETs are observed to have about 1 dB higher gain under the 5 V drain bias, 15 dBm input power conditions. With 8 V drain bias the conventional MESFETs have about 20% higher output power with 4 dB gain, but at the highest drain voltages the SIGFETs have significantly higher output powers than MESFETs because their output power does not saturate so

rapidly with drain voltage. This is assumed to be due to the higher gate breakdown voltage.

Some of these results are illustrated by the data in Table 4, which gives some of the dc and rf properties of SIGFETs from slices having several different doping levels. Also included are data (when available) from conventional MESFETs fabricated from the same slice. The dependence of microwave performance on epitaxial doping level is similar to that of MESFETs,[6] with the highest powers obtained with devices having $n \sim 8 \times 10^{16}$, but with a broad range of doping levels producing good performance. There is no indication of superior performance of heavily doped devices as suggested by Pruniaux, et al.[3] The microwave performance of the most heavily doped devices is not as good as that of some of the more lightly doped devices. For purposes of comparison, the maximum output powers with 4 dB gain at 8 GHz plotted as a function of drain bias are illustrated in Figure 14 for a SIGFET and a MESFET with 2400 μm gate widths. With 8 V drain bias the MESFET has significantly higher output power, but it saturates at 11 V drain bias, while the SIGFET continues to increase. The highest output power observed with a 2400 μm gate width SIGFET is 2.69 W with 4 dB gain at 8 GHz. This is 1.12 W/mm gate width and is higher than for any MESFET yet fabricated. This output power occurred with 15 V drain bias and saturated at that voltage, probably due to device heating. Extensive thermal measurements on both SIGFETs and MESFETs indicate a thermal resistance of 35 to 40°C/W (2400 μm gate width). At 15 V drain bias the active regions of the device in question were probably 150 to 200°C, which would lead to about 1.5 dB gain degradation.

The SIGFETs exhibited impressive performances at higher frequencies as well. With 15 V drain bias values up to 1.1 W at 4 dB gain were obtained at 11 GHz. It is possible that the reduced gate capacitance (C_g) due to the semi-insulating layer contributes to the improvements in the high frequency performance. Although this layer also reduces the transconductance (g_m), it

Table 4

Performance of 2400 μm Gate Width GaAs SIGFETs and Companion MESFETs

Slice Number	Type	Epitaxial Doping Level ($\times 10^{16}$) (cm^{-3})	Transconductance (for 300 μm Gate Width) (mmho)	8 GHz Microwave Performance: Gain P_{in} = 15 dBm $V_{ds} \approx 5$ V (dB)	8 GHz Microwave Performance: P_{out} with 4 dB Gain V_{ds} = 8 V (W)	8 GHz Microwave Performance: Maximum P_{out} with 4 dB Gain (W)	Drain Bias (V)
PM7-64	SIGFET	5.5	14	6.2	1.10	2.40	15
PM7-63	MESFET	5.5	17	7.0	1.32	1.91	13
PM7-66	SIGFET	14	19	5.9	1.29	1.78	11
PM7-69	SIGFET	11	16	6.5	1.18	1.82	14
PM7-68	MESFET	11	27	7.4	1.38	1.59	11
PM7-73	SIGFET	4.5	13	5.6	0.98	--	--
PM7-72	MESFET	4.5	16	7.3	1.15	--	--
PM7-84	SIGFET	7	19	5.8	1.29	2.69	15

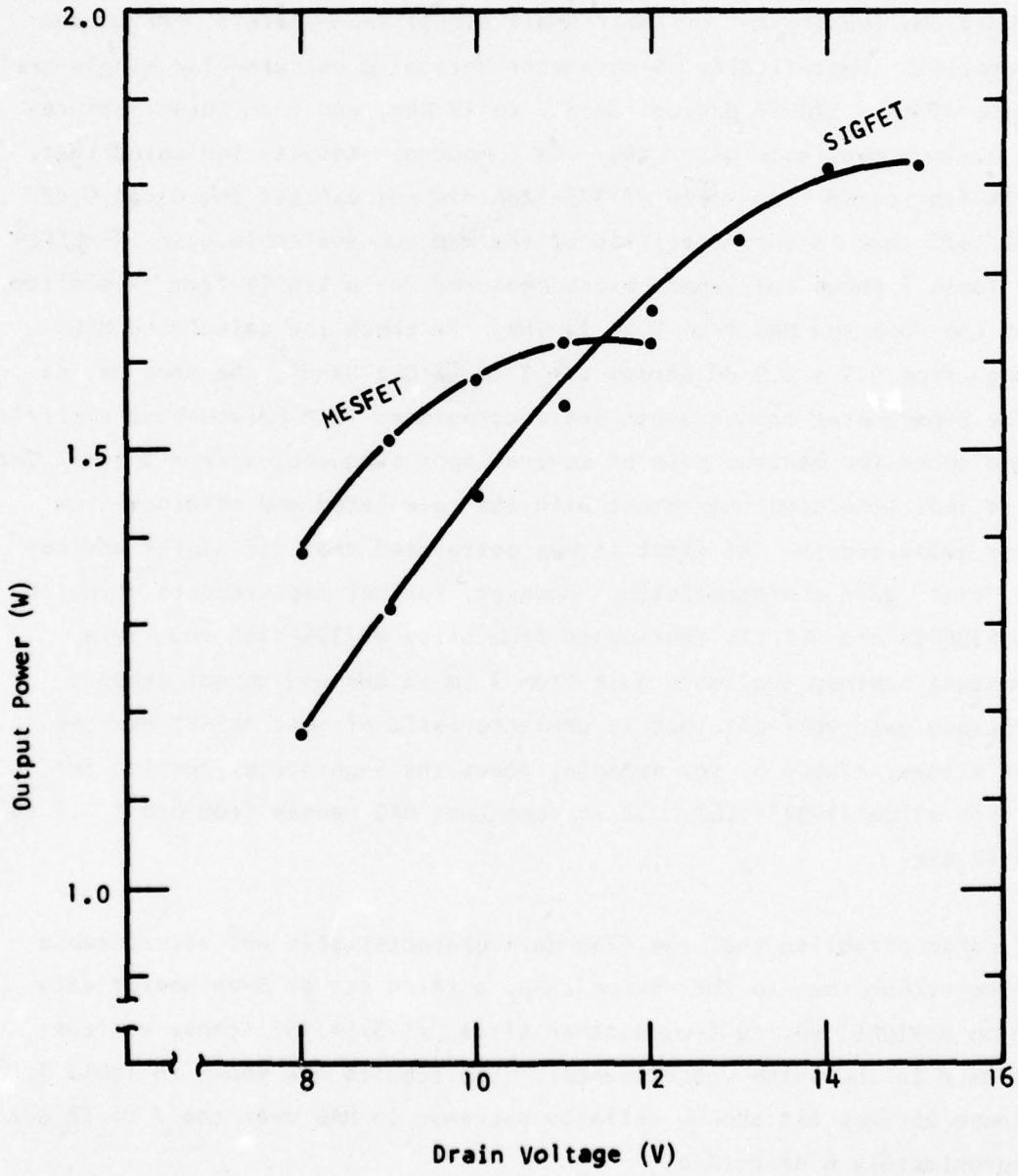


Figure 14 Maximum Output Power at 8 GHz with 4 dB gain as a Function of Drain Bias for a 2400 μm Gate Width SIGFET and a MESFET Fabricated from the Same Slice

decreases C_g even more, so that the net effect is an increase in the ratio, g_m/C_g, which favorably influences the high frequency characteristics of FETs.

Comparison of the rf characteristics of SIGFET and MESFET devices also included the measurement of their small signal S-parameters, for common source operation. Specifically, S-parameter data were measured for single-cell (600 μm gate width) SIGFET devices from 7 to 12 GHz, and from these measurements the maximum available gain, MAG, was computed. Results indicated that the SIGFETs fabricated from slice #17375-126A did not exhibit the usual 6 dB/octave roll-off that is characteristic of the maximum available gain in MESFET devices. Table 5 shows the S-parameters measured for a SIGFET from this slice, as well as the computed MAG from 7 to 12 GHz. To check the calculated MAG (which range from 5.5 ± 0.9 dB across the 7 to 12 GHz band), the same device used in the S-parameter measurements was incorporated in a narrow-band amplifier circuit and tuned for maximum gain at several spot frequencies from 7 to 12 GHz. The results indicated close agreement with the calculated MAG obtained from S-parameter measurements. At first it was postulated that all SIGFET devices have this "flat" gain characteristic. However, further measurements revealed that both SIGFETs and MESFETs fabricated from slice #17375-126A show this fairly constant maximum available gain from 7 to 12 GHz and do not exhibit the 6 dB/octave gain roll-off that is characteristic of most MESFET devices from other slices. Table 6, for example, shows the S-parameter results for a MESFET from slice #17375-126A. It is seen that MAG ranges from 6.8 ± 1.0 dB from 7 to 12 GHz.

To further establish that the flat gain characteristic was attributable to the slice rather than to the device type, a third set of S-parameter data was taken on a SIGFET device from another slice, #17375-105I (those devices were also used in the pulse measurements). The results are shown in Table 7. Indeed, these devices did show a definite decrease in MAG over the 7 to 12 GHz range, approximately 6 dB/octave.

Table 5

Measured S-Parameters of a Single-Cell (600 μm Gate Width) SIGFET for Common Source Operation from Slice #17375-126A

Frequency (GHz)	Mag (dB)	S_{11} Magnitude/θ°	S_{12} Magnitude/θ°	S_{21} Magnitude/θ°	S_{22} Magnitude/θ°
7.00	5.8	0.740/-115	0.048/50	0.970/64	0.650/-53
7.50	6.2	0.740/-121	0.055/52	0.990/59	0.660/-47
8.00	6.0	0.730/-131	0.053/50	0.990/50	0.660/-52
8.50	5.9	0.715/-139	0.058/54	0.990/45	0.665/-45
9.00	5.2	0.725/-149	0.059/54	0.870/40	0.675/-51
9.50	4.7	0.710/-156	0.059/55	0.860/36	0.660/-52
10.00	5.2	0.720/-159	0.062/62	0.900/32	0.640/-50
10.50	5.1	0.720/-162	0.071/63	0.890/24	0.635/-53
11.00	4.8	0.710/-162	0.079/60	0.880/21	0.620/-59
11.50	6.1	0.730/-179	0.084/58	0.980/14	0.580/-68
12.00	6.4	0.720/180	0.098/70	0.960/9	0.590/-73

SIGFET: One-Cell (600 μm Gate Width, 2.0 μm Gate Length) from Slice #17375-126A. Bias Conditions: V_D = 7.0 V, I_D = 175 mA, V_c = 1.6

Table 6

Measured S-Parameters of a Single-Cell (600 μm Gate Width)
MESFET for Common Source Operation from Slice #17375-126A

Frequency (GHz)	Mag (dB)	S_{11} Magnitude/θ°	S_{12} Magnitude/θ°	S_{21} Magnitude/θ°	S_{22} Magnitude/θ°
7.0	7.0	0.79/-105	0.040/52	1.00/68	0.68/-37
7.5	7.6	0.80/-103	0.046/62	1.10/66	0.65/-25
8.0	7.5	0.78/-111	0.045/56	1.10/54	0.67/-38
8.5	7.8	0.74/-114	0.052/58	1.21/50	0.68/-38
9.0	7.5	0.74/-125	0.056/58	1.10/42	0.70/-48
9.5	6.2	0.73/-124	0.057/59	1.00/33	0.69/-50
10.0	6.3	0.73/-140	0.056/65	1.00/28	0.68/-46
10.5	7.1	0.75/-147	0.063/64	1.00/22	0.70/-48
11.0	5.8	0.73/-152	0.071/65	0.95/18	0.67/-41
11.5	6.6	0.77/-162	0.075/69	1.00/5	0.62/-40
12.0	7.1	0.76/-154	0.083/72	1.05/-2	0.65/-48

MESFET: One-Cell (600 μm Gate Width, 2.0 μm Gate Length) from Slice #17375-126A. Bias Conditions: V_D = 7.1 V, I_D = 174 mA, V_G = -3.8 V

Table 7

Measured S-Parameters of a Single-Cell (600 μm Gate Width)
SIGFET for Common Source Operation from Slice #17375-105I

Frequency (GHz)	Mag (dB)	S_{11} Magnitude/θ°	S_{12} Magnitude/θ°	S_{21} Magnitude/θ°	S_{22} Magnitude/θ°
7.0	7.6	0.74/-138	0.066/18	1.22/50	0.62/-64
7.5	7.7	0.76/-140	0.075/17	1.20/46	0.61/-62
8.0	6.4	0.74/-149	0.064/15	1.06/36	0.64/-72
8.5	6.7	0.72/-152	0.066/15	1.10/30	0.67/-70
9.0	6.2	0.72/-158	0.067/16	1.00/31	0.68/-74
9.5	4.8	0.67/-160	0.068/19	0.93/28	0.67/-72
10.0	4.6	0.64/-169	0.070/19	0.97/18	0.65/-70
10.5	5.2	0.67/-179	0.076/13	1.00/11	0.65/-75
11.0	4.2	0.67/177	0.080/13	0.94/11	0.60/-78
11.5	3.6	0.62/175	0.080/13	0.98/-4	0.55/-84
12.0	3.3	0.63/172	0.082/16	0.92/-8	0.55/-91

SIGFET: One-Cell (600 μm Gate Width, 2.0 μm Gate Length) from Slice #17375-105I. Bias Conditions: V_D = 7.0 V, I_D = 70 mA, V_G = -1.0 V

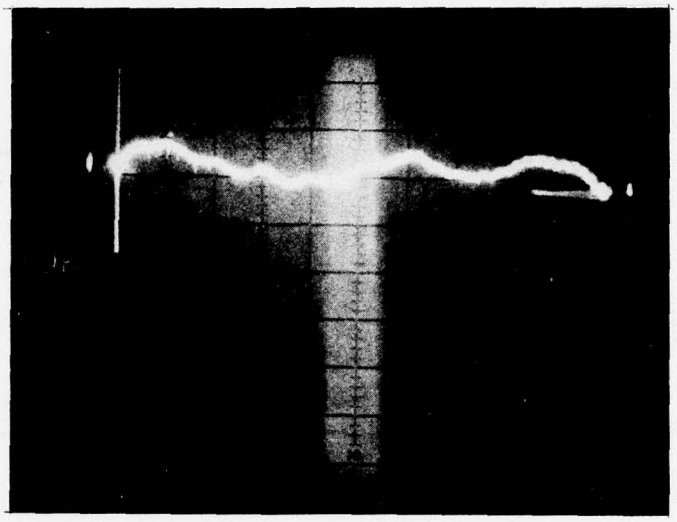
From the measurements performed it can be concluded that the relatively flat MAG characteristic is exhibited by both MESFET and SIGFET devices from slice #17375-126A. However, this is not characteristic of other slices, and SIGFETs do not generally exhibit a flat gain characteristic. In fact, the evidence suggests that SIGFETs and MESFETs fabricated from the same slice have similar S-parameters. Indeed, a 7.4 to 12.4 GHz SIGFET amplifier with a gain of 5.5 dB ± 1 dB was developed using a single-cell device with a total width of 600 μm. The gain vs frequency characteristic of this amplifier is shown in Figure 15. The circuit design was actually based on S-parameters measured from a one-cell MESFET fabricated from the same epitaxial wafer (16375-30IIA). This indicates that the presence of a semi-insulating layer beneath the gate of an FET does not produce a major perturbation in the characteristics of amplifiers produced from such devices.

SIGFET devices were also tested for microwave gain as a function of the implant parameters. The devices were tested at 8.0 GHz under two conditions: 15 dBm input power at 5 V_{SD}, and 20 dBm input power at 8 V_{SD}. Only single cells were tested. The devices were tuned for maximum gain using tuning chips on the microstrip circuit, using slide-screw tuners, and by adjusting gate bias. These data are presented in Figure 16. Considering the wide variation in gain observed at constant implant conditions, there is little evidence here that gain is dependent on implant conditions within the range tested.

Epitaxial SIGFETs were also microwave-tested in the same manner and exibited gains (4 to 7 dB) equivalent to those of the ion implant produced SIGFETs.

2. Pulsed Operation

SIGFETs and MESFETs from the same slice were operated under pulsed conditions at high drain voltages and rf input power. SIGFET and MESFET one-cell devices (with 600 μm gate widths and 2 μm gate lengths) were tuned up as



Vertical: 2.5 dB/div

Horizontal: 500 MHz/div
(7.4 GHz to 12.4 GHz)

SIGFET: Single Cell (600 μm gate width)
Bias: V_D = 5 V, I_D = 149 mA,
V_G = -1.1 V

Figure 15 A 7.4 to 12.4 GHz SIGFET Single-Stage Amplifier with 5 dB Small Signal Gain

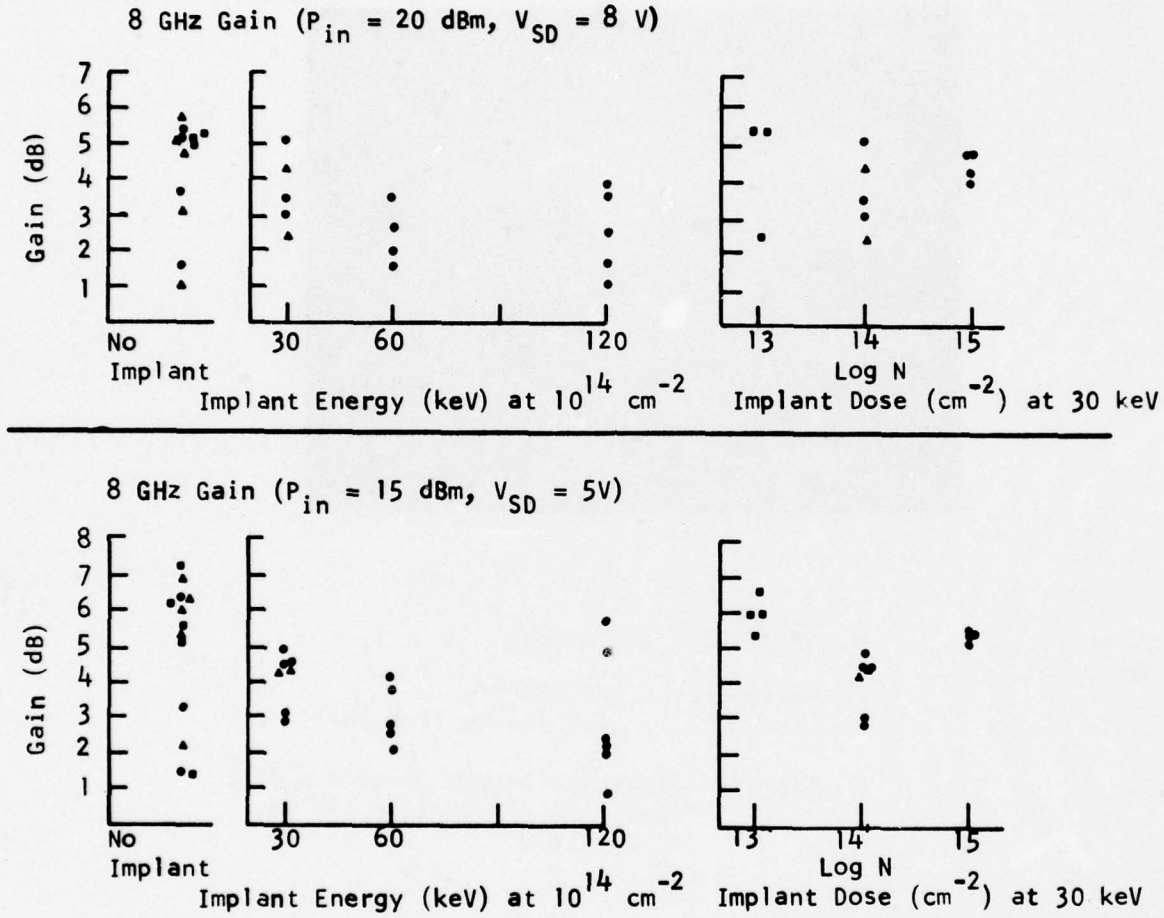


Figure 16 Microwave Gain of SIGFET Devices as a Function of Ar^+ Implant Energy and Dosage

narrow-band amplifiers at 9 GHz and pulsed (by pulse biasing the gate voltage) for pulse lengths of about 0.5 μs and for duty cycles less than 1%.

The purpose of the tests was twofold: first, to determine whether the maximum dc drain voltage applied to the device (i.e., before failure) can be extended to higher values under short pulse operation; and second, if so, to determine if the SIGFET (or MESFET) has an advantage over the other type of device in power output during pulsed operation.

Evaluation of the FET amplifier under pulsed conditions has been performed using a pulse biasing scheme that pulses the gate from the pinchoff condition to the nominal gate bias. The input rf is applied as a cw signal, while the output of the FET amplifier pulses on and off according to the gate bias. The drain voltage is maintained at the same level during the ON and OFF portion of the cycle.

Figure 17 shows the measuring system for the pulse measurements. A cw source such as a sweeper/TWTA combination provides the input signal to the FET amplifier under test. The gate pulsing circuit generates the proper level and polarity for the gate signal. It is driven by an HP 214A pulse generator. The rest of the system consists of standard calibration and power-monitoring equipment for measuring gain under cw and pulsed conditions. A crystal detector (HP 8470B) is used to display the output power on the oscilloscope. The scope is also used to monitor the gate voltage. The detector output is calibrated under cw conditions using the precision attenuator and power meters without the amplifier under test. After the detector is calibrated, the test amplifier is inserted, and a cw power reference datum is established on the CRT screen. During pulsed operation, the relative power of the pulsed output can be compared with this cw datum.

All the devices were tuned initially under cw conditions at 9 GHz with a drain voltage of 7 V and the gate voltage adjusted for maximum power.

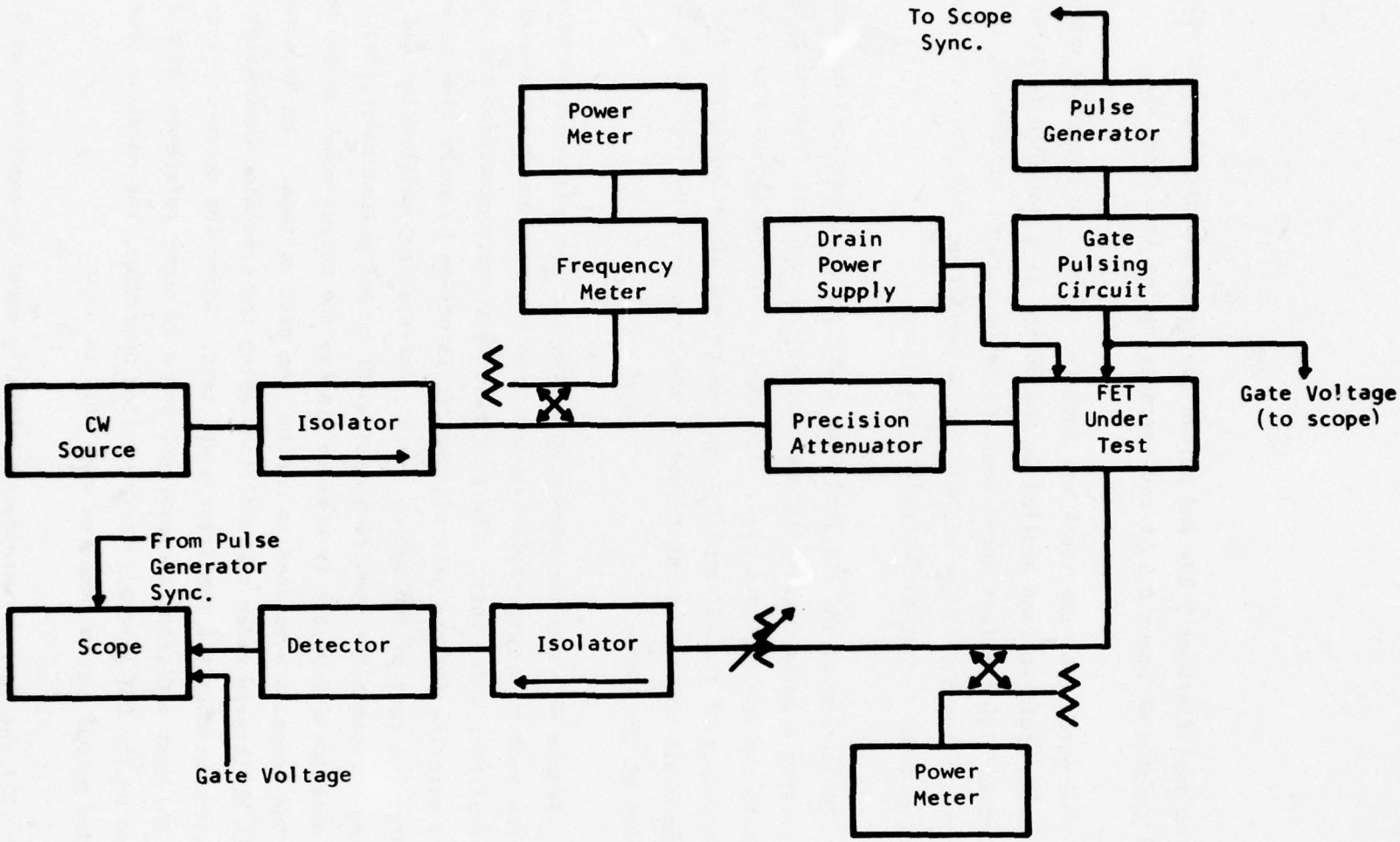
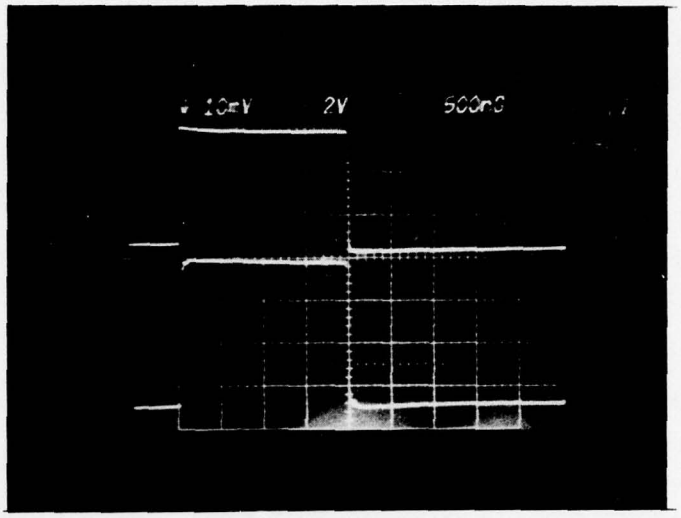


Figure 17 Pulse Measurement Set-Up for FETs

The dc gate bias was then adjusted for pinch-off and a pulse applied to the gate to turn on the transistor. The drain voltage was then increased, and the rf power during the pulse was monitored and recorded. Retuning of the device for maximum power was also performed at the different drain voltages.

The first set of pulse experiments was performed on eight SIGFET devices and three MESFET devices fabricated from the same slice. The slice was chosen because it yielded good devices (i.e., devices of both types exhibited rf gain and power output comparable to the best of the MESFETs fabricated up to that time), which were easily tuned up as narrowband amplifiers at 9.0 GHz. Of the eight SIGFET devices, six operated pulsed mode at drain voltages of 17 to 19 V. Two of the SIGFETs failed at lower voltages. All three MESFET devices failed when the drain voltage approached 14 V. For both types of devices, an increase in power was observed with increased drain voltage, as expected. For example, at 16 dBm of input power a SIGFET exhibited 4.7 dB gain, while at 18 V, 5.9 dB was observed. This same device showed a 5 dB gain at 20 dBm of input power; however, a MESFET at the same input power level exhibited 6 dB gain at 7 V of drain voltage and 7.9 dB gain at a voltage of 14 V. It was also observed that at the 18 V drain voltage this SIGFET failed when the pulse length was increased from 0.5 μs to 10 μs and 10% duty cycle. This is most probably due to an increase in device temperature as the pulse length approaches and exceeds the thermal time constant of the device chip. It is for this reason that succeeding measurements made during high drain voltage operation were done only in the short pulse mode. Figure 18 shows a photograph of the oscilloscope display of the output power pulse, indicated as "Detector Output" (upper trace), and the corresponding gate voltage pulse (lower trace), for the SIGFET pulse operated at 18 V drain bias, with the pulse length increased to 2 μs. The second horizontal graticule line from the top corresponds to an output power of 25 dBm. The $\pm$ 1 dB marks at the right of the screen indicate the detector calibration for that level of output power. For this device the gate voltage corresponding to maximum output power is nearly zero, as seen in the lower trace. Very little amplitude droop ($<$ 0.2 dB) is observed



Vertical - upper trace: 2 dB/div (between ± 1 dB marks)
- lower trace: 2 V/div

Horizontal: 200 nsec/div
Input Power: 20 dBM
Gain (during on period): 5 dB
Duty Cycle: ≈ 2.4%
Bias Condition: $V_D \approx 18$ V
$V_G \cong 0$ V (during on period)
Frequency: 9.0 GHz
SIGFET: 1 cell (600 μm gate width, 2.0 μm gate length) from slice 17375-105I.

Figure 18 Pulse Response of a SIGFET Operated at a Drain Voltage of 18 V

in the output pulse. However, when the pulse width was increased to about 10 μs, the device failed.

Based on these initial observations, further experiments were planned to investigate the power saturation characteristics of MESFETs and SIGFETs operated at high drain voltages. Specifically, these experiments were to answer the question, "Does the SIGFET have any power advantage over the MESFET for short pulse, high drain voltage operation?" The pulse experiments were carried out in a manner similar to that described above.

Figures 19 and 20 show a typical set of power-added versus input power characteristics for one-cell SIGFETs operated at drain voltages up to 18 V. The 4 dB gain points for a given drain voltage are indicated by triangles. In both cases significant increase in power-added occurs up to about 14 V, while beyond 14 V only $\frac{1}{2}$ dB additional increase in the power-added is observed at a drain voltage of 18 V. The peak of the power-added curves occurs at about 21 dBm of input power with about 4.9 dB gain. Also shown are the corresponding cw data taken at the lower drain voltages. Typically, a difference between cw and pulsed data for both SIGFETs and MESFETs occurs at drain voltages of 10 V and higher, while for smaller drain voltages, little or no difference is observed.

Figure 21 shows similar data for a typical one-cell MESFET. Although the MESFETs cannot be operated much beyond 14 V drain voltage, it is seen that the maximum power-added is at least comparable and, for the device shown in Figure 21, is indeed higher than for the SIGFET devices. The MESFET curves also show much higher gain at low input powers in Figure 21. However, other MESFET devices from the same slice have shown small signal gains comparable to the SIGFET curves, although the tendency is typically for higher gains for MESFETs at all input levels.

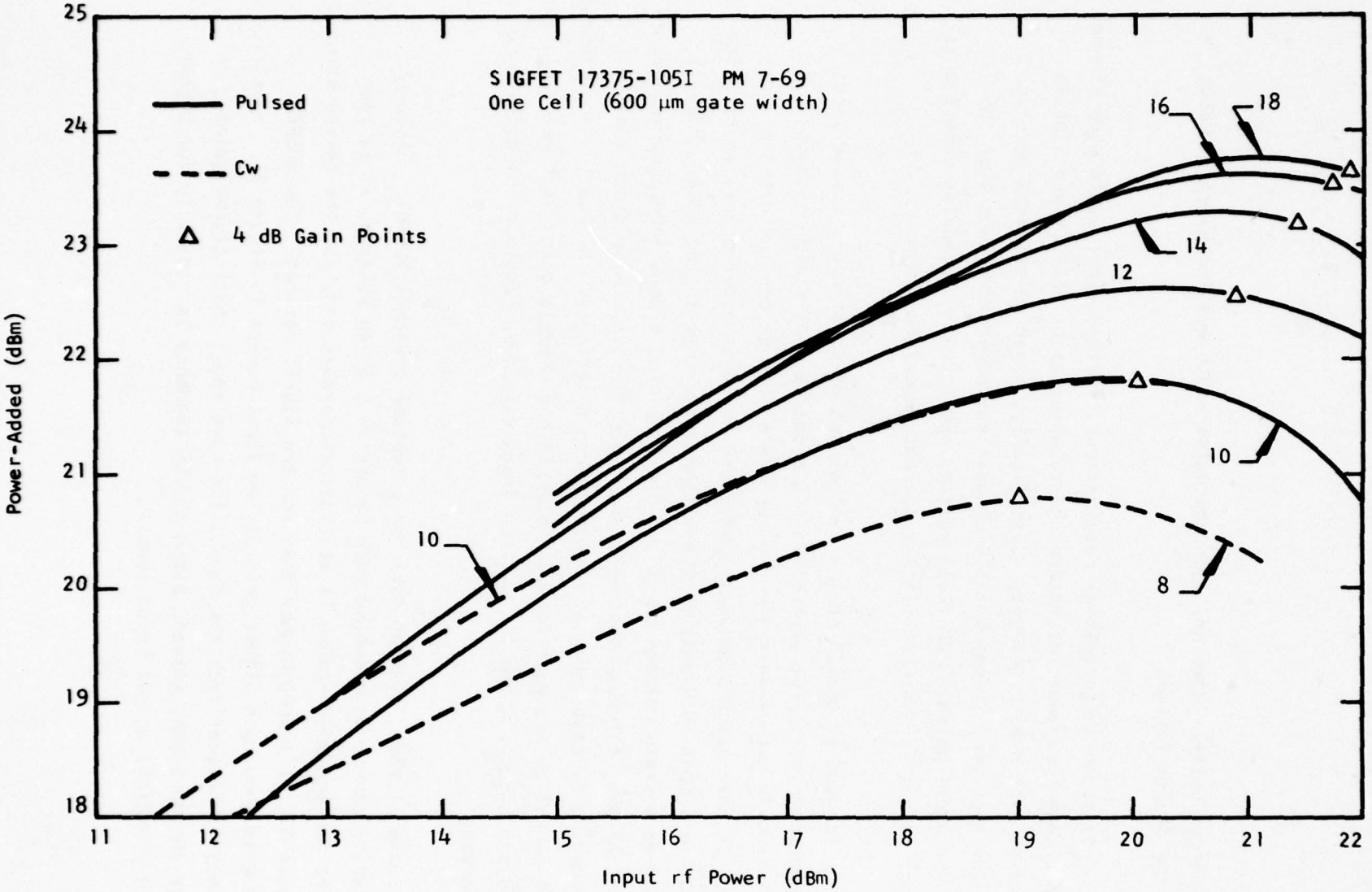


Figure 19 Power Saturation Characteristic of SIGFET Device A at 9.0 GHz.

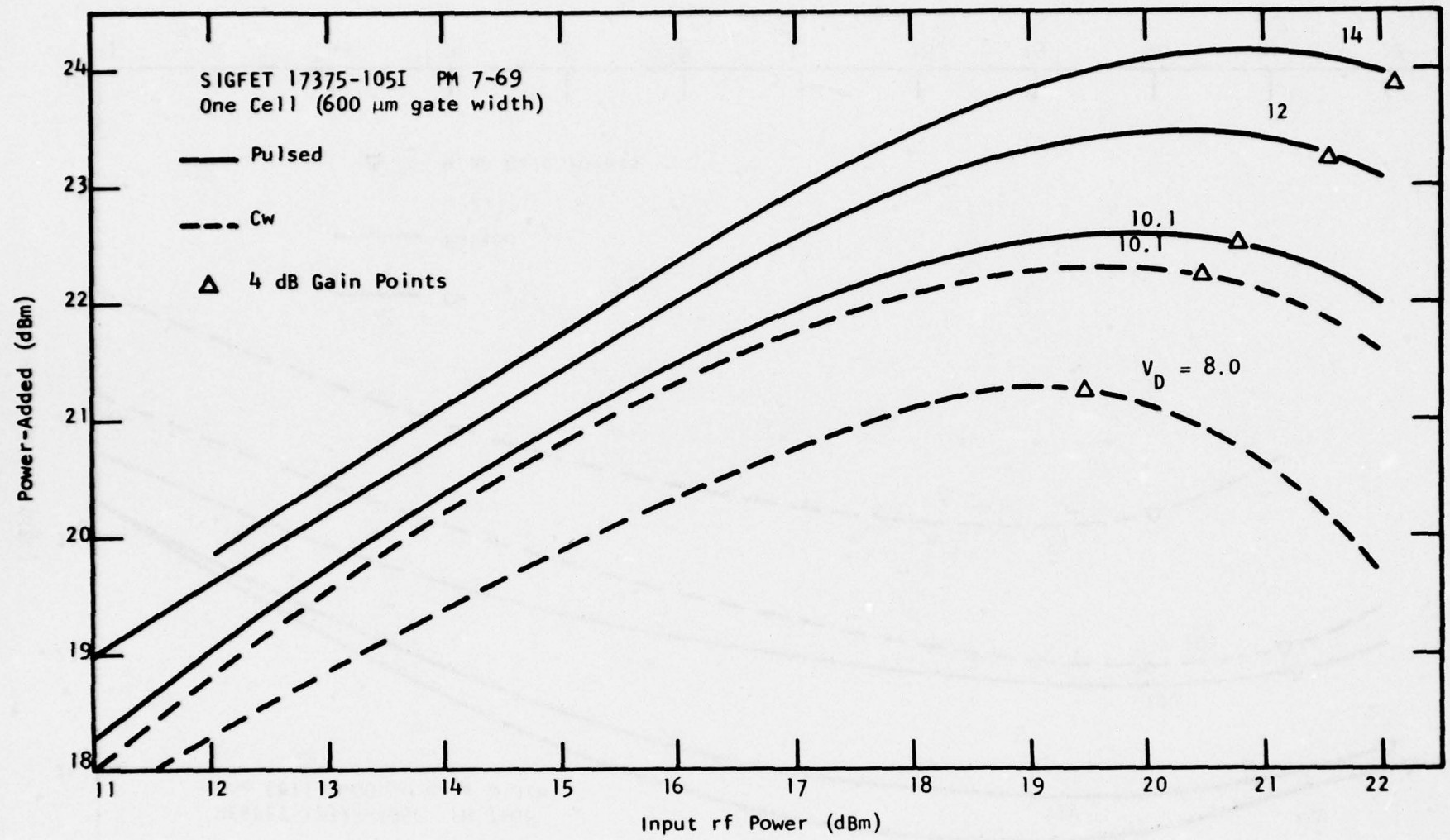


Figure 20 Power Saturation Characteristic of SIGFET Device B at 9.0 GHz.

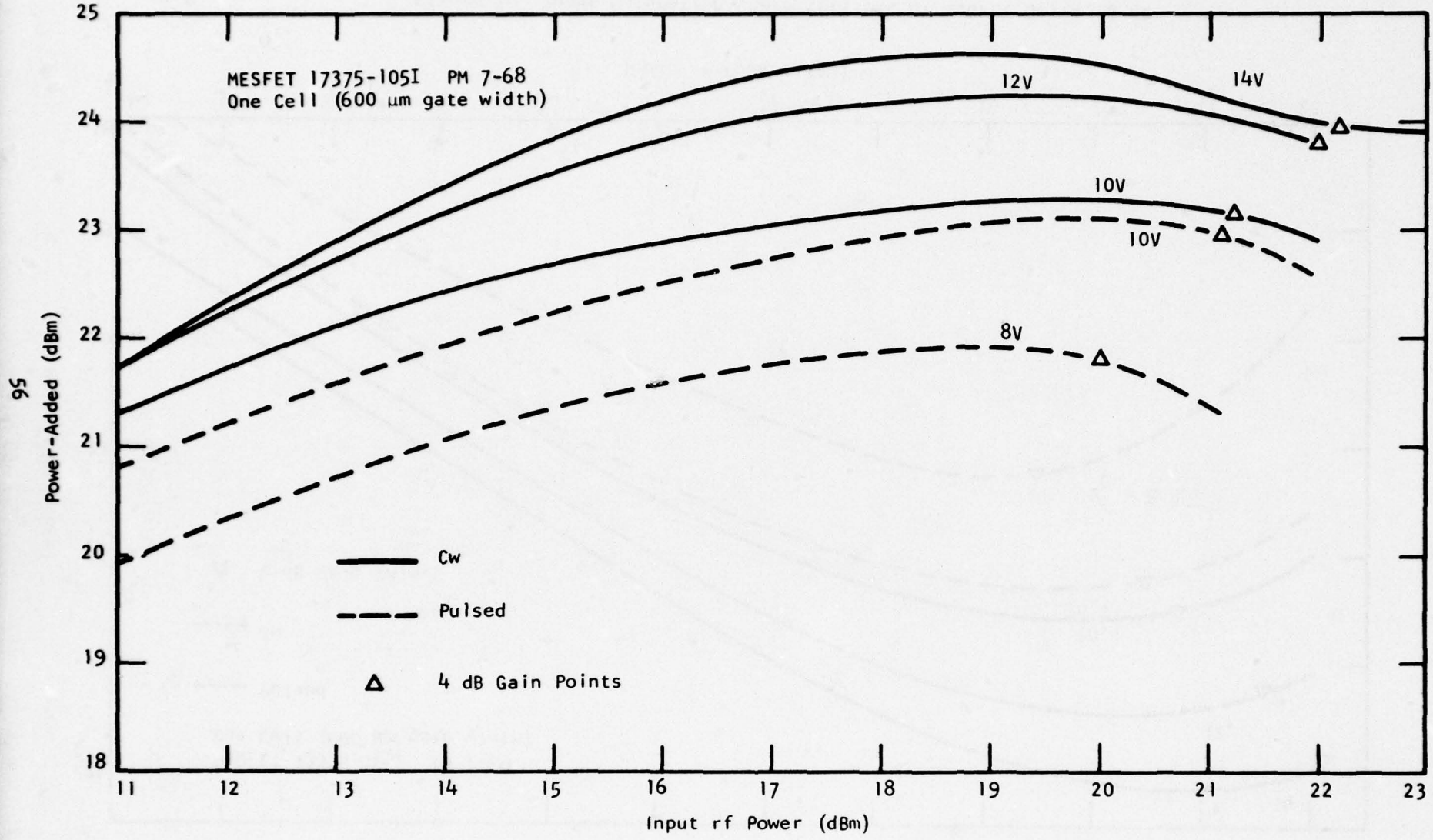


Figure 21 Power Saturation Characteristic of MESFET Device at 9.0 GHz.

Pulse measurement results for the one-cell SIGFETs and MESFETs investigated indicate no apparent advantage in power output for the SIGFET over the MESFET device under short pulse operation (where heating of the device during the on time is kept low compared to cw operation). This is true even in light of the fact that the SIGFET device is capable of sustaining significantly higher drain voltages during short pulse operation.

SECTION V
n^+ CONTACT TECHNOLOGY

The n^+ contacts are used with GaAs FETs principally because they permit device operation at higher drain voltages without avalanche breakdown at the drain contact and catastrophic device failure.[7,8] This is essential if full advantage is to be taken of the SIGFET's high gate breakdown voltage. n^+ contacts may also provide more reliable operation of lower drain voltages. There should also be a reduction in contact resistance with n^+ contacts, but the contact resistance is already quite low and the resulting improvement in device microwave performance would be small.

An additional benefit of using n^+ contacts is the promise of an improved noise figure. Theoretical work has indicated that when an FET is tuned for minimum noise figure, the parasitic resistances may contribute nearly half of the noise.[9] Furthermore, recent experiments have exhibited an improvement in noise figure when n^+ contacts are used.[10] These considerations apply especially to SIGFETs, since they inherently have an increased parasitic gate resistance.

A. Formation by Localized Ion Implantation

Procedures were investigated for formation of n^+ source/drain contact regions by ion implantation using patterned photoresist as a mask. In the first experiments a dosage of 1×10^{14} cm^{-2} 200 keV Se ions was locally implanted into the source/drain regions. Prior to the implant, these regions were lightly etched to identify the implanted regions during the subsequent processing steps. To avoid channeling, the ions were implanted 7° from the surface normal. After implantation, the photoresist was removed, and a protective Si_3N_4 film was deposited in preparation for annealing. Initially, the Si_3N_4 was deposited by a low-temperature, plasma-enhanced process. Unfortunately, these films cracked severely during a 30 minute, 825°C anneal in H_2, and the surface was so eroded that further processing was precluded.

Other slices, implanted under the same conditions, were subjected to nitride deposition using a 700°C pyrolytic SiH_4/NH_3 process previously developed at another TI facility. These slices were then successfully annealed under the same conditions with no apparent degradation of the Si_3N_4 or the underlying GaAs surface. With a successful nitride deposition process identified, the optimum annealing temperature could be examined.

Identification of the successful annealing conditions was made through the following experimental sequence: Epitaxial slices were cleaved into three portions, two of which were patterned with polymerized photoresist to expose source/drain regions. One of the patterned portions was subjected to ion implantation at the exposed areas, while the other was not implanted and served as a control. One-half of the remaining, unpatterned portion was covered with photoresist so that it would be protected while the other half was implanted. All implantation was done at room temperature using 10^{14} cm^{-2} 200 keV Se ions. After implantation (and resist removal), each portion was simultaneously capped with pyrolytic Si_3N_4 as described above and annealed under the conditions to be described. The degree of activation was evaluated from the source/drain resistances measured on the patterned portions, and the zero-bias capacitances and C-V doping profiles were measured with Al Schottky barriers deposited on the unpatterned portion.

The initial group was annealed at 825°C for 30 minutes. Afterwards, extremely large resistances were measured between the source and drain regions, indicating little activation of the implanted Se^+. The next series was given a more extensive anneal at 875°C for 45 minutes. In this case each portion, including the one that was not implanted, exhibited excessive leakage current, possibly due to surface contamination. Finally, detectable activation was achieved by annealing a group at 900°C for one hour in hydrogen. In this case, the source/drain resistance was reduced by 60% and the saturation current was increased by 50% as compared with the portion that was not implanted. However,

this series was not without problems. A very high doping level was observed at the surface of the unpatterned portion in the region protected by a sheet of photoresist, as well as in the region directly exposed to the ion beam. Apparently, the photoresist failed to protect the surface completely. As a result of this observation, single and double coatings of AZ 1350J photoresist, both baked (one hour at 37°C) and unbaked, were examined for their ability to protect against 200 keV Se^+ implants. All combinations proved inadequate except the one that used doubly coated and baked photoresist. This combination was found to provide reasonable surface protection.

After the above implant mask procedure was established, six slices were cleaved from a single larger slice that had been C-V profiled over its entire surface. Four of these slices were coated with baked, double-thickness photoresist over half their surfaces. The other two had source/drain contact windows, also defined by double-thickness photoresist. Of the first group of four slices, one was subjected to the complete implantation and activation procedure, which consisted of implantation of 200 keV Se^+ ions at a dosage of 10^{14} cm^{-2}, followed by capping with pyrolytic Si_3N_4 and a one-hour anneal at 900°C. None of the remaining three were subjected to implantation. Instead, one served as a control, another was capped only, and third was capped and annealed. They were evaluated by applying an Al dot pattern and measuring breakdown voltages and C-V profiles. The characteristics of the control and cap-only slice agreed. The anneal-only slice had a breakdown voltage less than 50% that of the control. Its C-V profile gave hints of a higher doping near the surface. The protected half of the implanted slice had characteristics roughly matching the anneal-only slice. The implanted half was ohmic, exhibiting little or no Schottky breakdown.

Of the second group of two slices with source-drain patterns, one was a control and one was subjected to implantation and activation. Both slices then had source-drain metallization applied and alloyed. The control slice showed a source-drain saturation current of 200 mA. The implanted slice showed a wide range of saturation current, varying across the slice between 80 and > 400 mA.

Measurements from test areas in the parts of this slice with high currents showed smaller contact resistance and lower channel resistivity than did the parts with lower currents, or the control slice.

It is inferred from the above that, although some surface conversion did occur during annealing, significant in-depth activation was being obtained with a corresponding reduction in contact resistance.

At this stage it was decided to also try Si^+ implantation, and special gas valves and other equipment required for a silane source were installed. Silicon was then implanted at 120 keV, 10^{14} cm^{-2}. After capping with pyrolytic silicon nitride, these slices were annealed at 900°C for one hour in a hydrogen atmosphere. Comparison of the reverse breakdown voltages of Al Schottky barriers applied to the control and implanted slices revealed that significant activation had been achieved. However, further examination showed an increased source-drain resistance on the slice that was implanted in the source-drain regions. Alternate annealing procedures were examined in an effort to minimize the wide variation in results previously encountered from run to run. Much of the variation has been attributed to the influence of the Si_3N_4 capping layer used to protect the slices during the high temperature anneal. With this in mind, two "capless" anneal procedures were examined. In each case the slices were annealed for 20 minutes at 800°C in a hydrogen stream with an appropriate arsenic overpressure. In one procedure the overpressure was provided by a solid, single crystal GaAs ingot placed upstream and at a slightly higher temperature than the slices being annealed. This procedure was later rejected because the slices suffered surface degradation as evidenced by the appearance of a haze due to the presence of small pits on the surface. Subsequent electrical evaluation revealed an order of magnitude decrease in surface carrier concentration, increased source/drain resistance, and poor contact resistance.

In the other procedure the overpressure was provided by a boat containing gallium previously saturated with arsenic at a temperature in excess of the

anneal temperature. Once again, the boat was located upstream from the slices. This approach produced no surface degradation. The electrical results were somewhat contradictory. A point-by-point C-V profile taken using a capacitance bridge showed no change in doping profile. However, no results were obtainable from an automatic C-V profiler, and the source/drain characteristics were extremely resistive.

An additional set of slices was implanted with 120 keV Si^+ (dosage of 1×10^{14} cm^{-2}) and annealed in the conventional manner using a pyrolytic Si_3N_4 capping layer. The capping layer cracked extensively during the 900°C anneal; however, a sufficient amount of undamaged area remained to permit evaluation of the extent of activation. In this case, activation was achieved near the surface, resulting in a doping level greater than 7×10^{17} cm^{-3}. However, the doping profile decreased rapidly as a function of depth and was less than 1×10^{16} cm^{-3} at a depth of 0.18 μm. Source/drain characteristics were extremely resistive. Finally, a slice that was implanted with Si at 5×10^{13} cm^{-2}, 120 keV, and capped and annealed by the normal procedure also exhibited increased source-drain resistance.

A summary of the implant activities is presented in Table 8. In general, evidence of activation is often observed, at least very near the surface, on slices that are uniformly implanted and evaluated by Schottky breakdown voltage, zero-bias capacitance, of C-V profiling. On the other hand, the companion slices that were implanted only in source-drain regions with subsequent metallization and alloying usually exhibited increased source-drain resistance and lower saturation current. A possible explanation for this unexpected behavior is that during the alloying process, the alloy and regrowth region extends beyond the region of enhanced carrier concentration. Thus, the contact metal alloys deeper than the implanted region to form a contact/semiconductor interface in the unimplanted material having a normal carrier concentration. The alloy depth has been shown[11] to be $\sim$ 0.1 μm for the conditions employed, which is

Table 8

Summary of n^+ Implant Activities

Species	Energy (keV)	Dose (cm^{-2})	Anneal Conditions			EVALUATION: Source-Drain I-V Characteristic Compared to Unimplanted Control Slice	EVALUATION: Evaluation from Breakdown Voltage of Schottky Barriers
Se	200	10^{14}	S_3N_4 (1)	30 min	825°C	Surface eroded due to S_3N_4 film cracking	
Se	200	10^{14}	S_3N_4	30 min	825°C	Highly resistive	Nearly ohmic
Se	200	10^{14}	S_3N_4	45 min	875°C	No change, but leaky	Nearly ohmic
Se	200	10^{14}	S_3N_4	60 min	900°C	Less resistive	Nearly ohmic
Se	200	10^{14}	S_3N_4	60 min	900°C	More resistive	No evaluation
Se (2)	200	10^{14}	S_3N_4	60 min	900°C	Variable: Less to more resistive	Nearly ohmic
Si (2)	120	10^{14}	S_3N_4	60 min	900°C	More resistive	Slight activation
Si (2)	120	2×10^{13}	Capless (Solid GaAs Ingot)	20 min	800°C	More resistive	Decreased carrier concentration
Si (2)	120	2×10^{13}	Capless (Saturated Ga Source)	20 min	800°C	Highly resistive	No change
Si (2)	120	1×10^{14}	S_3N_4	60 min	900°C	Highly resistive	Activation near surface (5×10^{17})
Si (2)	120	5×10^{13}	S_3N_4	60 min	900°C	More resistive	Little or no activation

(1) Low temperature plasma deposited; all others pyrolytic

(2) Doubly coated and baked photoresist used for implant mask

approximately equivalent to the 0.1025 μm projected range of 120 keV Si^+ ions. However, the activated region is reported to extend to approximately 0.2 μm after annealing under similar conditions.[12] Furthermore, the measured resistances were actually greater than those generally obtained for contacts alloyed directly into conventional 1×10^{17} cm^{-3} material.

It is also possible that the optimum alloying conditions determined for conventional material are different from those suitable for n^+ material. This possibility is supported by the observation that alloyed contacts to n^+ epitaxial layers exhibited a wider variation in their properites than contacts alloyed under the same conditions to conventional epitaxial layers. This effect will be discussed in more detail in a later section.

Finally, due to equipment limitations, all implants were made into unheated slices. Implantation at elevated temperatures is known to be desirable, particularly for Se^+ implants into GaAs.[13] Due to extensive residual lattice damage, some of the implant experiments may have increased the activated carrier density to a lesser degree than the resulting mobility degradations. Thus, enhanced carrier concentrations would be indicated by C-V measurements, but the overall resistivity of the material would not have increased as expected.

In general, although carrier activation was demonstrated in several ion implantation experiments, the results were highly variable. The variability could be due to a number of possible factors such as variations in the properties of the capping layers, the annealing conditions, or the alloying process. However, detailed examination of these factors was beyond the scope of the program. Fortunately, more consistent results were obtained by formation of n^+ contact layers through sequential epitaxial growth.

2. Formation by Epitaxial Growth

To provide an alternate, and possibly more reliable means for formation of n^+ contact regions, an epitaxial growth system was modified to permit deposition of n^+ contact layers. In this approach three epitaxial layers are grown sequentially on the semi-insulating substrate. The first is an undoped, high resistivity buffer layer. This is followed by the active n layer and finally by the n^+ contact layer doped between 5×10^{17} and 2×10^{18} cm^{-3}. A doping profile from a slice grown in this manner is given in Figure 22.

FETs were fabricated from this material using two different procedures. Both are essentially the normal fabrication process with only a few variations. In each case, the entire slice is etched to reduce the n^+ layer thickness if it is excessively thick. Even so, rather high mesas are required because the presence of the n^+ layer precludes anodic oxidation (see below), and thus the n layers are thicker than those of anodically thinned slices. The extra thick n layer and the n^+ layer combine to form an active structure appreciably thicker than the single, thinned n layer of a normal MESFET and require formation of higher mesas. The large mesa height resulted in broken gate stripes as they crossed the mesa edge during the first attempts to process n^+ material. The problem was alleviated by development of a new mesa etchant composition that produces mesas with more gently sloped sides. The etchant, composed of 1 M NaOH, concentrated H_2O_2, and H_2O at a ratio of 23:4:10 by volume, eliminated the gate breakage problem.

Attempts to use the self-limiting anodic etching technique with a mask in order to selectively thin the slice only in the gate area (leaving n^+ material under the source and drain regions) were unsuccessful, because the anodic oxidation process rapidly undercuts the mask. Material near the surface, but under the mask, is removed laterally at a rate exceeding the removal rate in the desired vertical direction.

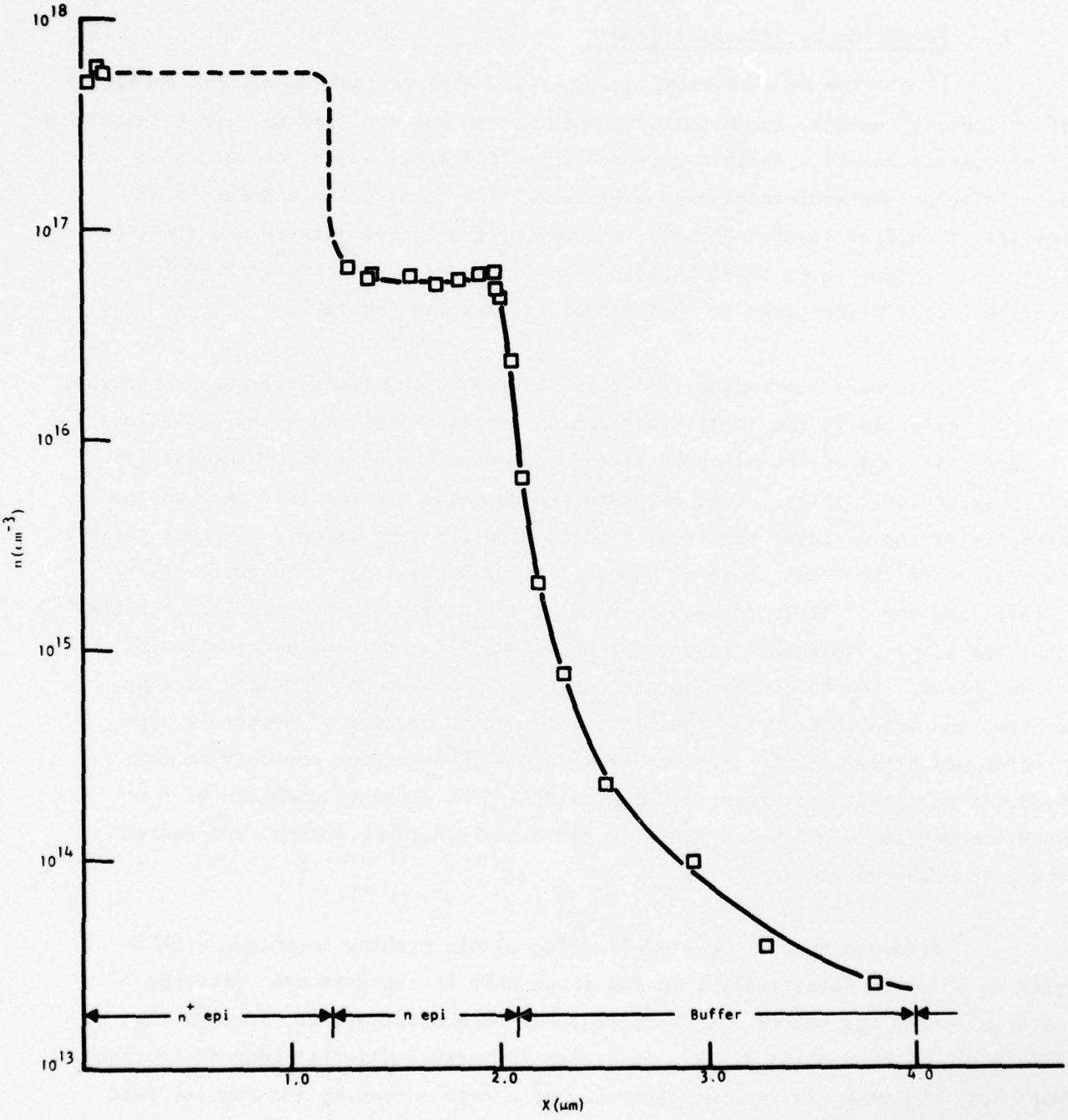


Figure 22 C-V Doping Profile of a Slice with an n^+ Epitaxial Layer. Dashed region surmised from cross section layer thickness measurements.

After etching the slice to the correct n^+ thickness and formation of gently sloped mesas, processing continues in one of two ways. In method one, the normal fabrication procedure is followed, but the gate recess step is used to recess the gate entirely through the n^+ layer and into the active n layer. As usual, the optimum depth is determined by monitoring the source-drain current. Further processing is normal.

The second fabrication procedure, designated method two, is a self-aligned gate process in which the photoresist defining the gate is also used as an etch mask. An etchant is then used to etch through the n^+ layer and undercut the photoresist, resulting in the structure indicated in Figure 23(a). Subsequent gate evaporation and lift-off produce the structure in Figure 23(b). Initial evaluation of this procedure using substrate material was quite successful for defining both 2 μm and 1 μm gate geometries. The mask used to apply the source-drain pattern has a source-drain spacing larger than normal. This allows a noncritical placement of the gate mask pattern, since the actual source or drain edge will be essentially the n^+ material remaining after the gate etch [Figure 23(b)]. After this step, processing proceeds normally. Figures 24 and 25 show SEM photographs of the gate area (including the mesa edge crossover) of devices fabricated using methods one and two, respectively. The protective nitride coating that normally covers the gate area has been etched away to allow a better view of the gate recess. Note that even though these mesas are twice as high as conventional mesas, the gate coverage across the step is excellent. The slope of the mesa edge appears steeper than it actually is (approximately 35° from horizontal) due to the angle at which the photographs were taken. The very wide source-drain metallization spacing that allows a noncritical placement of the gate mask in method two is evident in Figure 25.

Neither fabrication procedure yielded results that were clearly superior to the other, and both have yielded FETs with excellent dc and microwave characteristics. For example, single-cell structures with a 600 μm x 2 μm gate

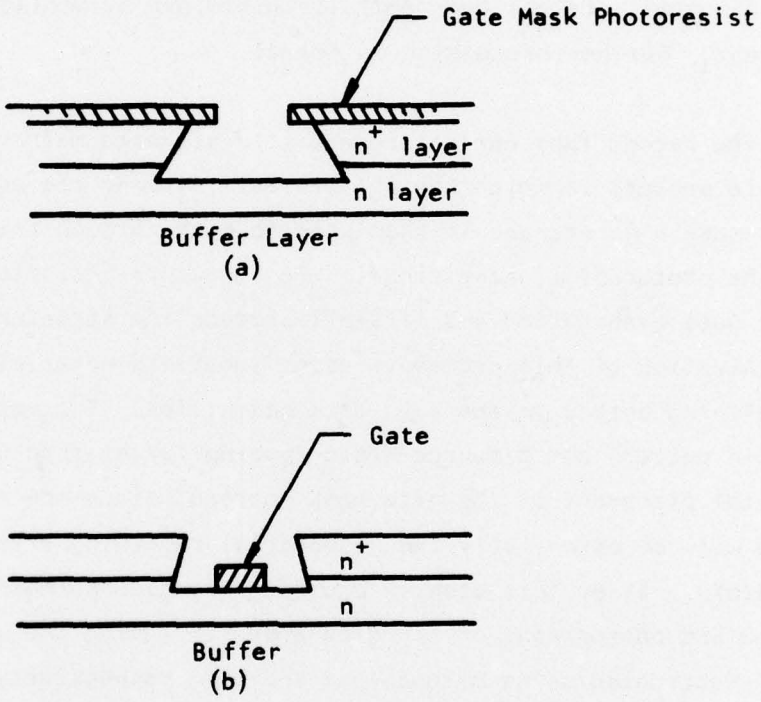


Figure 23 Self-Aligned Gate Procedures Using Undercut Photoresist on an n^+ Epitaxial layer

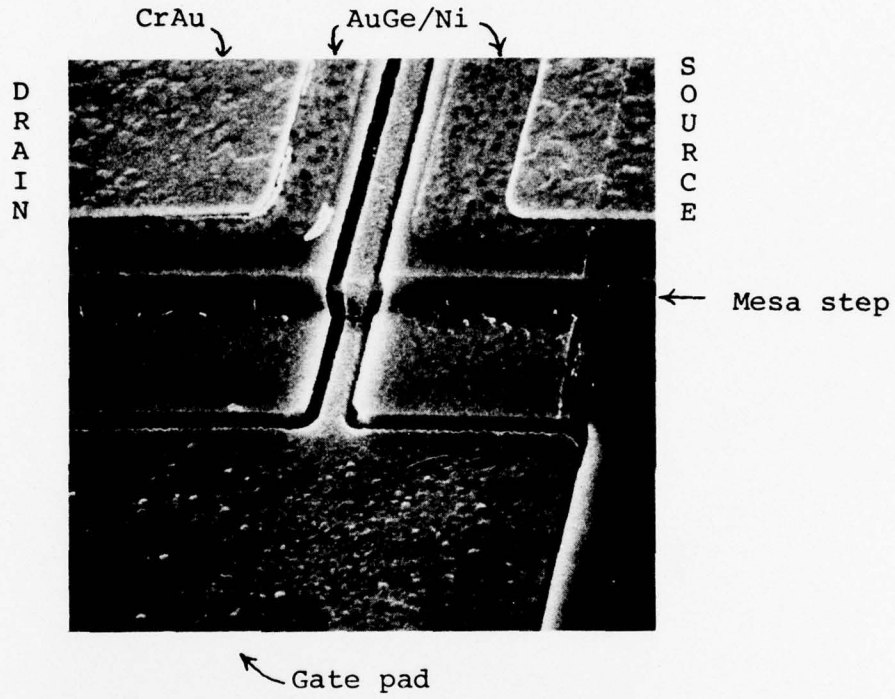
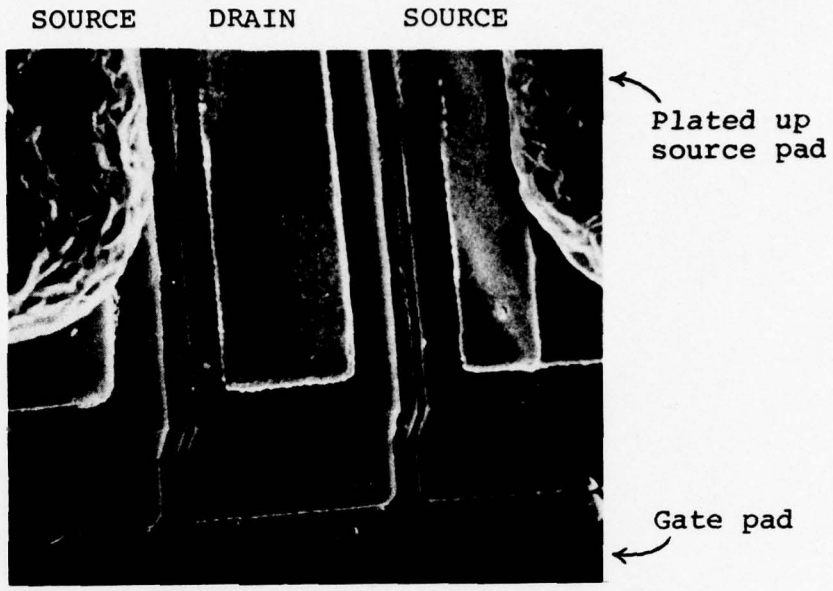


Figure 24 SEM Photograph of the Gate Metallization of an FET Fabricated from n^+ Epitaxial Material Using Method One (see Text). The gate has been recessed entirely through the n^+ layer into the n layer.



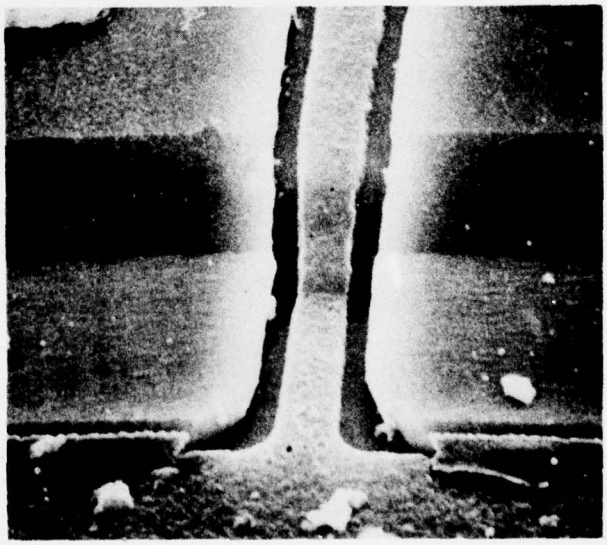


Figure 25 SEM Photographs of the Gate Metallization of an FET Fabricated from n^+ Epitaxial Material Using Method Two (See Text). The gate has been recessed entirely through the n^+ layer and into the n layer.

distributed over four fingers have produced gains greater than 6 dB when tested at 8 GHz with 15 dBm input power and 5 V_{SD}. At 0 dBm input power, gains greater than 9 dB were obtained. This compares favorably with the results obtained from good MESFETs produced with the same mask set or material without the epitaxial n^+ layer.

The source-drain burnout voltage of these devices was of major interest, since an ability to operate under large source-drain bias was the principal motivation for using n^+ contacts. Devices from several n^+ slices were tested, and all exhibited source-drain burnout voltages between 26 and 30 V when operated with a moderate (2 to 4 V) gate bias. This is a significant improvement over the 12 to 18 V range exhibited by MESFETs lacking n^+ contacts and fabricated using the same mark set. Further measurements made using test structures from the above n^+ slices showed the expected decrease in contact resistance. However, this decrease was not as large as anticipated. The contact resistance, R_c, is given by

$$R_c = \frac{1}{Z} \sqrt{\frac{r_c \rho}{a}},$$

where Z is the width of the contact, r_c the specific contact resistance, ρ the resistivity of the GaAs material under the contact, and a the thickness of the GaAs material between the alloyed contact and the buffer. Hence, for the structures with n^+ layers discribed above, both the extra thickness of the active layer and its decreased average resistivity should contribute to a decreased contact resistance. However, the improvement was less than would have been predicted from either the increased thickness or the decreased resistivity alone. It was as though the specific contact resistance, r_c, was worse in these slices than in conventional material without n^+ layers.

This observation, together with the difficulty experienced in reducing the contact resistance with localized ion implantation, suggested a closer examination of the quality of the Au/Ge/Ni ohmic contact to heavily doped

material. For this purpose, two types of investigations were initiated: (1) An examination of contact resistance in heavily doped material as a function of alloy temperature, and (2) examination of contact resistance in an extra thick, normally doped n layer.

The first experiment was designed to determine whether the optimum alloy conditions for conventional n layers (450°C, 60 s), were also optimum for alloying into material doped an order of magnitude higher. Source-drain metallization was applied to a slice having an n^+ layer doped at 10^{18} cm^{-3}. This slice was then cleaved into several parts for alloying at different temperatures for 60 seconds. Previous experiments[11] on normally doped layers had exhibited virtually no dependence on alloy time. It was visually observed that alloying occurred for pieces alloyed at 400°C and at 425°C. However, at 450°C the first sample appeared to "overalloy," as evidenced by an increased surface roughness of the AuGe/Ni. Experience has shown that overalloying leads to inferior contacts. A second slice with approximately the same doping was used to repeat the experiment. This slice, in contrast to the previous slice, showed no overalloying, even up to 500°C, and subsequent contact resistance measurements showed a minimum over the range 425°C to 450°C. Furthermore, these minimum values (approximately 0.06 Ω for a width of 1 mm) were appreciably better than those obtained on the previous slices with n^+ layers. Indeed, the values were better than would have been predicted from either the increased thickness or reduced resistivity alone, but still not as good as would be expected considering both thickness and resistivity.

The second experiment, using a slice with an extra thick, normally doped ($\sim 10^{17}$ cm^{-3}) layer, also yielded contact resistances that were slightly better than predicted on the basis of its increased thickness. Devices from this slice were tested for source-drain burnout and exhibited values of approximately 23 V. Although this value is not as good as that obtained using the n^+ devices, it is better than that of FETs with normal doping and thickness.

In general, the experiments suggest that the improvements observed in contact resistances of devices fabricated from slices with n^+ layers are due largely to the increased GaAs thickness beneath the contact, while the improvements in source-drain burnout voltage are due to both increased thickness and decreased resistivity. Furthermore, the variation in the quality of the alloyed contacts in highly doped material appears to be significantly greater than that observed for conventional material.

SECTION VI

CONCLUSIONS AND RECOMMENDATIONS

Theoretical analysis of the dc and rf operating characteristics of Class A and Class B FET amplifiers revealed that maximum efficiency is expected for Class B operation into a tuned load. This conclusion was supported by the experimental observation that maximum efficiency was obtained for GaAs FETs when the gate bias approached the pinchoff voltage, i.e., approaching Class B operation. However, for Class B operation the ratio of gate breakdown voltage to the pinchoff voltage should be relatively high, such as might be obtained with FETs having insulated gates (IGFETs) or semi-insulated gates (SIGFETs). Procedures were developed to fabricate GaAs SIGFETs using localized ion bombardment to form the region of high resistivity or semi-insulating GaAs beneath the gate contact metal. By use of 30 keV Ar^+ ions at a dosage of 1×10^{14} cm^{-2}, an approximately 0.2 μm semi-insulating region is formed. The resulting GaAs SIGFETs have higher gate breakdown voltages and greater ratios of gate breakdown voltage to pinchoff voltage than conventional GaAs MESFETs fabricated from the same slice. Additional evaluation revealed that in comparison with MESFETs, the SIGFETs exhibit lower transconductances and $\sim$ 1 dB less small signal gains, but at high drain voltages the increased gate breakdown voltage contributes to greater output powers. Furthermore, the power saturation of SIGFETs occurs at greater drain voltages. However, due both to device heating and to avalanche phenomena at the drain contacts, it is difficult to exploit the high gate breakdown voltages of the SIGFETs. Under short pulse operations the SIGFETs are capable of sustaining greater drain voltages before failure than the companion MESFETs. However, the overall powers delivered by the two basic device types under pulse operation are comparable. Under cw conditions one SIGFET delivered the highest output power (2.7 W) of any 2400 μm gate width GaAs FET at 8 GHz, yet this value has now been approached by a MESFET which yielded 2.6 W.

To fully exploit the GaAs SIGFET, it is necessary to develop a reliable n^+ contacting technology. Using Se^+ and Si^+ ion implantation, techniques were

developed that resulted in significant activation and enhanced carrier concentrations. However, when applied to the formation of localized n^+ contact regions, the resulting contacts after alloying were more resistive than conventional contacts. Sequential epitaxial growth of n^+ contacting layers was shown to be a viable approach. Devices fabricated with the epitaxial n^+ contact layers were found to be capable of withstanding approximately twice the drain voltage before failure than conventional FETs without n^+ layers.

With respect to future activities, efforts designed to exploit innovative circuit techniques for Class B operation of FETs should be beneficial. The GaAs IGFET should be reconsidered in light of any major improvement in the characteristics of GaAs/insulator interfaces. Although for most applications the GaAs MESFET with its simplified fabrication procedure should be adequate, the greater reverse gate breakdown voltage of a GaAs SIGFET makes it attractive for Class B and other applications where large gate voltage swings are essential. Furthermore, since the SIGFET should particularly benefit from new developments in heat-sinking and n^+ contacting technology, its merits should be reappraised as improved FET processing procedures are introduced.

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APPENDIX

PUBLICATIONS

APPENDIX

PUBLICATIONS

The following paper was published for which credit was given under Contract No. N00014-75-C-1134:

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